

**TESTING AND CHARACTERIZATION OF HIGH-SPEED
SIGNALS USING INCOHERENT UNDERSAMPLING
DRIVEN SIGNAL RECONSTRUCTION ALGORITHMS**

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TESTING AND CHARACTERIZATION OF HIGH-SPEED SIGNALS USING INCOHERENT UNDERSAMPLING DRIVEN SIGNAL RECONSTRUCTION ALGORITHMS

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To myself,
my family, my friends and
Eun Jeong Cha,
the only person worthy of my company.

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SUMMARY

Signal reconstruction algorithms with sub-Nyquist sampling rate and low-cost hardware schemes for high-speed signal testing are proposed in this research. A new subsampling based dual-rate signal acquisition technique for a wideband sparse signal is presented. This work reconstructs the input signal without any front-end radio-frequency (RF) components such as mixers, local oscillators and filters. Practical issues on the dual-rate sampling hardware such as phase synchronization and channel mismatch calibration are discussed and resolved. A novel approach for the algorithmic clock-recovery and the jitter tracking of high-speed digital signal is also proposed. The contribution of this work is to perform the clock-recovery by incoherent subsampling without an external clock-data-recovery circuit, and therefore the hardware cost for testing the digital signal is reduced. Finally, the eye-monitoring and the self-calibration of high-speed transmitters by monobit-receivers are presented. Monitoring and adapting channel-behavior by the monobit-receivers significantly simplify the test architecture for multi-channel digital input/output (I/O).

CHAPTER I

INTRODUCTION

The proposed research will develop a framework for the signal reconstruction algorithms with sub-Nyquist sampling rate and the low-cost hardware schemes for testing in system level. A further objective of the proposed research is to monitor the device-under-test (DUT) and to adapt its behaviors. The proposed works are: 1) wideband signal reconstruction by dual-rate time-interleaved subsampling hardware and multicore signal reconstruction, 2) algorithmic clock recovery and jitter tracking by accurate period estimation with incoherent subsampling and 3) eye-monitoring and time-domain-reflectometry (TDR) by monobit-receiver signal reconstruction. The proposed work is summarized in Figure 1.

In the first work, the proposed architecture employs a combination of dual-rate

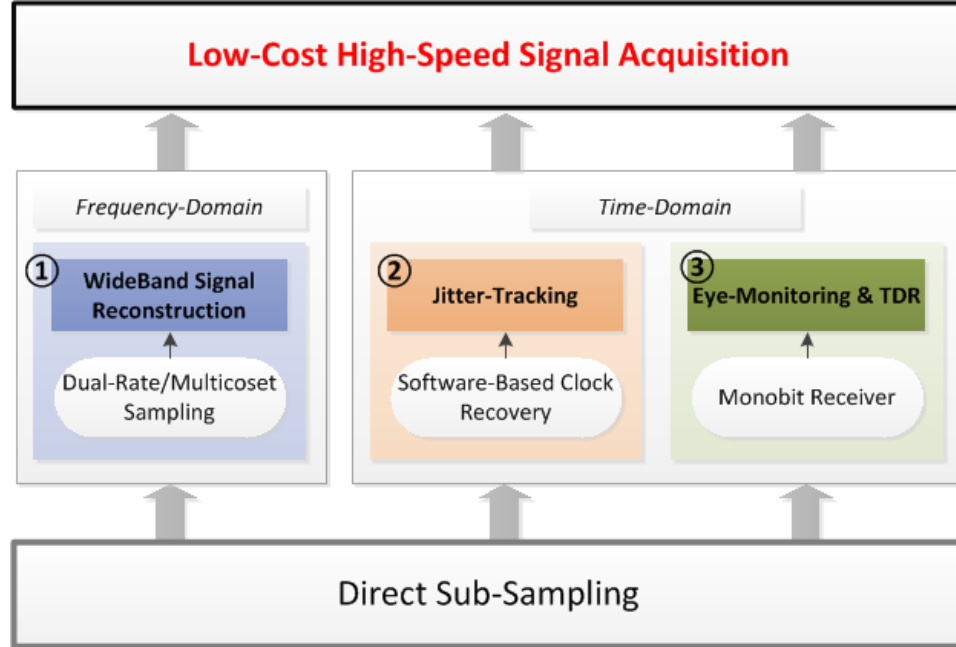


Figure 1: Summary of the proposed work.

time-interleaved subsampling hardware and associated multicore based back-end signal processing algorithms. In dual-rate sampling hardware, a pair of uniform samplers acquires a common incoming analog signal while the operation frequencies of the two samplers have a small frequency offset. Multicore signal reconstruction algorithm uses the re-sequenced nonequispaced samples of a frequency-sparse signal and achieves a signal reconstruction under certain conditions.

Second, a new algorithm to accurately estimate the fundamental period of a high-speed pseudo-random-bit-sequence (PRBS) using incoherent subsampling is proposed. The proposed incoherent subsampling method performs very accurate estimation of the fundamental period of the input signal enabling a time-domain signal reconstruction with very high signal-to-noise ratio (SNR). The proposed algorithm does not require additional hardware to synchronize the input signal frequency with the sampling clock frequency. As the clock-recovery is performed by software, we refer the proposed method as algorithmic clock-recovery.

Finally, low-cost multi-channel test architecture by monobit sampling is proposed. The proposed method uses a time-variant threshold voltage to increase its amplitude resolution. We propose two different architectures to test multi-channel digital IO; the first architecture is synchronized with the input test signal and the second one is not. The accuracy of the reconstruction is improved by proposed statistical estimation for monobit receiver. Using the monobit test architecture, we solve a problem of monitoring and adapting the channel behavior to enhance the signal integrity.

The following is the key contribution of this research.

- The wideband signal acquisition is done by direct subsampling. As the signal is directly sampled without any front-end radio-frequency (RF) components such as mixers or filters, the cost of hardware is reduced. Furthermore, the distortion and the nonlinearity from the RF components can be avoided. The combination of the dual-rate hardware and its designated discrete signal processing

algorithm, the spectrum of the wideband signal is perfectly reconstructed. We also present practical issues of the dual-rate sampling hardware such as phase synchronization and channel mismatch calibration.

- We propose an enhanced algorithmic clock-recovery of high-speed digital signal without using clock data recovery (CDR) circuits. As a result, a long-term jitter in the digital signal can be tracked and compensated.
- Low-cost multi-channel test architecture is proposed using monobit receiver and reconstruction algorithm. We present two different scenarios whether the system is in synchronization. The monobit signal reconstruction is further enhanced by statistical estimation. We also propose a new adaptive algorithm based on the monobit test architecture to perform the time-domain reflectometry (TDR) and to adapt the channel behavior for the signal integrity.

CHAPTER II

LITERATURE SURVEY

2.1 *Wideband Signal Acquisition*

The Whittaker, Kotelnikov and Shannon (WKS) theorem states that a signal band-limited to H Hertz can be reconstructed with $2H$ samples per second which is also known as the Nyquist rate [57]. However, as new multi-GHz digital circuits are designed and fabricated, high-speed signal acquisition and jitter analysis by conventional Nyquist rate sampling involve huge amounts of testing cost and is sometimes not even possible. When the signal is subsampled, the spectrum of the signal is aliased. Because of the spectral aliasing, the original information of the signal is distorted. The most advanced analog-digital-converter (ADC) in the commercial off-the-shelf (COTS) are running at maximum 3.6GSPS with 12-bit resolution [1, 33]. Therefore, it is difficult to characterize the spectrum beyond 1.8GHz bandwidth by the ADC.

Translating the frequency of the input signal to baseband is widely used in commercial spectrum analyzers to avoid the aliasing problem. Most modern spectrum

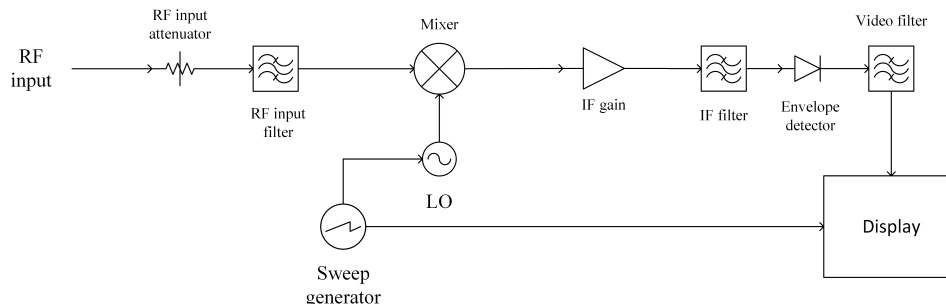


Figure 2: Block diagram of a superheterodyne spectrum analyzer [60].

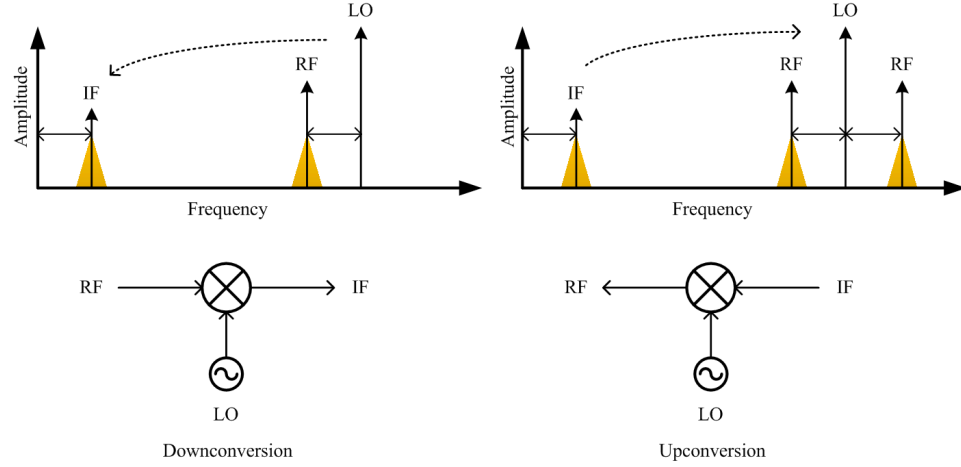


Figure 3: Downconversion and upconversion processes of mixer.

analyzers are superheterodyne, where heterodyne refers to mix and super means frequency above the audio range. In Figure 2, the block diagram of a superheterodyne spectrum analyzer is shown. The key idea is to mix the input signal with a tunable local oscillator resulting in downconversion of the input frequency to the intermediate-frequency (IF). As a result, the ADC at the final stage can satisfy the Nyquist criterion. Therefore, the performance of the spectrum analyzer is determined by its front-end RF circuits. In the next few paragraphs, a background theory and a practical design issue of the mixer will be addressed.

A frequency mixer is a 3-port RF circuit, where two ports are inputs and the other port is output. The mixer mixes the two input signal and generates the output signal so that its frequency is the sum and the difference of the inputs. In the spectrum analyzer, the desired output frequency of the mixer is lower frequency than the input signal frequency. Therefore, the two input ports are the input signal (RF) and the local oscillator (LO), and the output port is IF. In this setup, the mixer can downconvert the input signal (high frequency) into the IF signal (low frequency). In Figure 3, the downconversion and upconversion processes are illustrated in the frequency domain. When the RF port is used as an input and the desired output frequency is lower than its input frequency, the mixer performs a downconversion

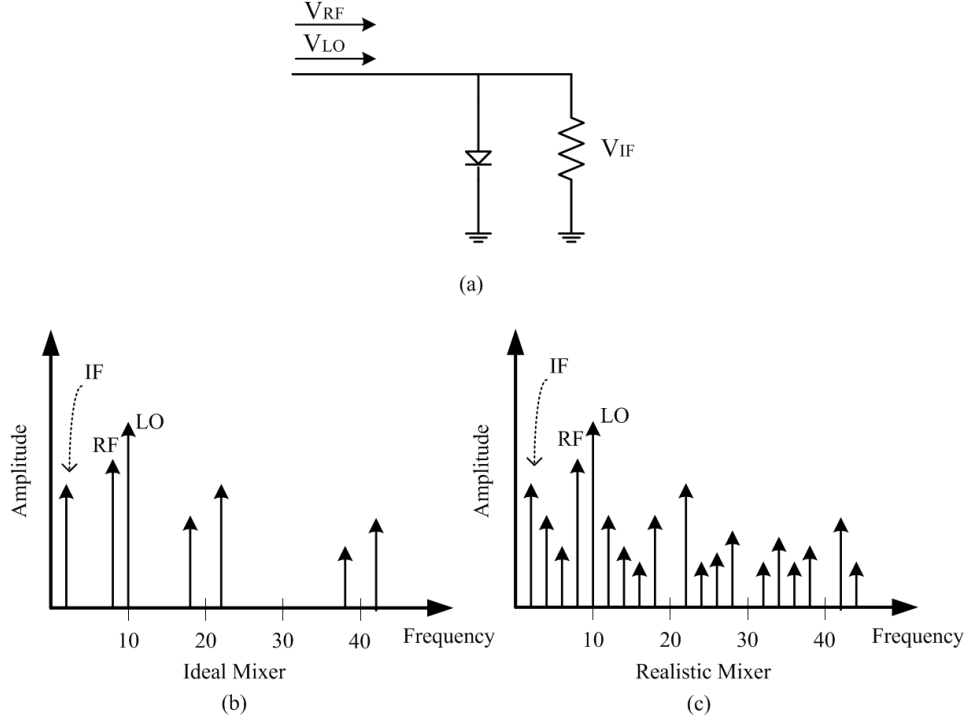


Figure 4: (a) A single diode mixer circuitry. (b) The spectrum of the ideal mixer. (c) The spectrum of the realistic mixer.

process. The LO frequency can be either higher or lower than the RF frequency as long as their difference keeps the desired IF frequency. When the LO frequency is below RF frequency, it is called low-side injection. Otherwise, it is called higher-side injection. When the RF port is an output and the IF port is an input, the mixer is in upconversion mode. In this case, the LO is used to upconvert the IF frequency to the RF frequency. Note that the image frequency of the IF appears on the low-side of the LO. Thus, the resulting RF signal contains a two-tone signal.

The modern mixer is designed by many different devices such as FET, CMOS and Schottky diodes. The FET and CMOS mixers are usually used in low-cost application where the performance is not critical, while the Schottky diode mixer can achieve higher performance. The simplest mixer scheme composed of a single diode is illustrated in Figure 4(a). A mixing process is driven by the LO signal assuming the RF signal is much weaker than the LO. As shown in Figure 2, the strength of the

input signal (or RF signal) is reduced by the RF input attenuator before the mixer. The small signal RF is chopped by the LO, which results in mixing with only odd harmonics of the LO in the perfect switching diode as shown in Figure 4(b). The frequency of the output IF is found as:

$$f_{IF} = k \cdot f_{LO} \pm f_{RF}, \quad (1)$$

where k is any odd integer. However, a realistic diode does not perform a perfect switching. Its I-V curve characteristic necessarily includes a transition region. In addition, the small signal RF will also contribute the switching process. These non-ideal combination causes extra mixing products. Therefore, the output frequencies of the IF results from mixing of all the harmonics of the RF and LO as follow:

$$f_{IF} = k \cdot f_{LO} \pm l \cdot f_{RF}, \quad (2)$$

where k and l are any integers. Compared to the spectrum of the ideal mixer, the realistic mixer creates more harmonic products in its output (Figure 4(c)). Since the expected downconverted signal by the mixer is only at $|f_{LO} - f_{RF}|$, the additional signals produced by the harmonics will cause problems. The research about high-performance mixers, RF filters and low-noise amplifiers (LNA) is developed to reduce the additional mixing products and images [53, 56, 69, 71]. In the superheterodyne spectrum analyzer, the IF filter selects the desired mixing products and rejects all other signals.

To summarize the mixer-based wideband signal acquisition, a wideband input signal is downconverted with the LO by the mixer so that the IF signal satisfies the Nyquist criterion. As the realistic mixer creates unwanted products, acquiring the desired signal involves a lot of RF circuits to pre- and post-process the input and the IF signals. These additional RF components and design efforts are the major part of the cost to develop a wideband signal acquisition system. In the next sections, prior works about different approach than the mixer-based one will be discussed.

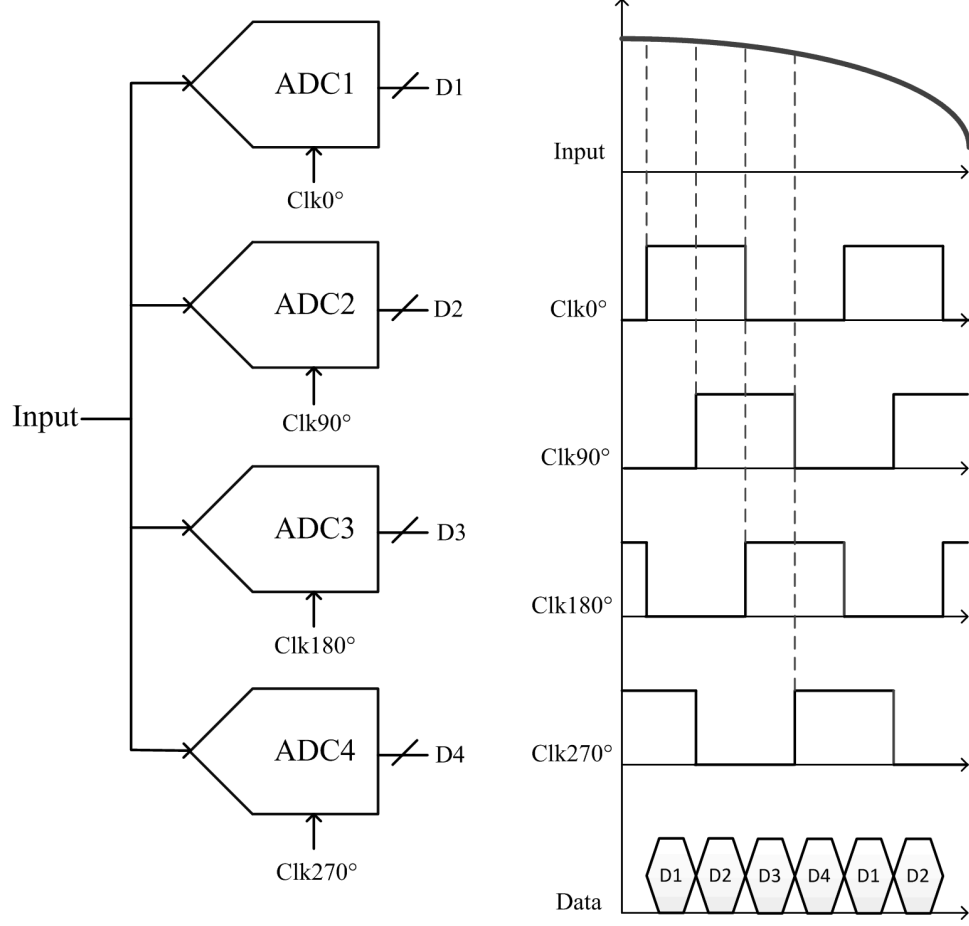


Figure 5: Block diagram of TIADC system and clock relationship.

One approach is to use multi-sampling channels in which a sampling rate in a single channel is sub-Nyquist rate but the overall system is above the Nyquist rate. This approach belongs to real-time sampling category because the final reconstructed signal is effectively based on the real-time samples at the Nyquist rate. Time-interleaved ADC (TIADC) utilizes M parallel channel ADCs running at a sampling rate of $1/M$ the overall system sampling rate [7, 8, 14, 37, 48, 62]. The sampling clock for each ADC is time-delayed so that the final output data stream merged by the M individual channel is equally time-spaced and has the equivalent samples as a single ADC sampling at full rate. Compared to a single ADC at full sampling rate, each channel of the TIADC does not fulfill the Nyquist rate. However, the overall sampling rate after merging the digital samples from M ADCs fulfills the Nyquist rate. In Figure 5,

four channel time-interleaved ADCs are illustrated. The phase of each sampling clock is shifted by 90 degree. The overall data rate of the system will be four time faster than a single ADC.

In the recent extended research of the TIADC, non-uniform sampling has been shown to be a more efficient method to acquire high-frequency signal components that are sparse in a certain domain (mostly in the frequency domain) than uniform sampling. Non-equispaced undersampling techniques have been investigated for the purpose of digitally enhancing the time resolution of sampling-based measurement systems given upper limits of their sampling rates by associated signal reconstruction algorithms. By this method, a faster effective sampling rate can be achieved compared to the sampling rate by the conventional time-interleaved sampling methods. Such a technique is used for the acquisition of high-frequency signal components that are sufficiently sparse in the frequency domain.

Nonequispaced undersampling requires a certain degree of modification to the existing sampling hardware. For example, periodic non-uniform undersampling (multicoset sampling) uses multiple sampling devices configured in a parallel architecture that acquires a common analog input signal. Each sampling device uses the same sampling frequency but different phases, individually acquiring a common analog input signal at nonequispaced phases. The key point in this scheme is that the sampling clocks running at the same rate have non-uniform initial phases [40, 67, 68]. In a typical way, the non-uniform phases of the sampling clocks are assumed to be implemented in hardware by delay circuits. In a similar reconstruction algorithm researched in [41], a random demodulator composed of a frequency mixer with a pseudo-random bit generator is used instead of non-uniform sampling scheme. However, those additional hardware components (delay circuits and random demodulators) introduce extra measurement noise to the sampling system due to additional jitter noise from the circuits themselves and the modulation signals.

To overcome the extra measurement noise issues caused by the customized non-uniform undersampling hardware described above, a multi-rate time-interleaved undersampling technique is introduced in [17, 21, 52]. In the multi-rate time-interleaved sampling approaches, a pair of uniform samplers acquires a common incoming analog signal while the sampling frequencies of the two samplers have a small frequency offset. Due to the sampling frequency offset, the time grids of the samples obtained from the two samplers are irregularly spaced. The obtained irregular sampling grid may not be as random as the one obtained by the random samplers described above, but such irregularly spaced samples can be used for the signal reconstruction with digital signal processing algorithms originally described for non-uniform sample sets with customized data pre-processing.

However, such signal reconstruction algorithms are hard to implement in digital signal processing devices due to their complexity, and the multi-rate sampling hardware still requires multiple high-speed samplers (if not on the order of 10) and their synchronization, which is an additional burden on system design or the potential cause of increased sampling noise in hardware. In many blind reconstruction works, the combination of sparse sensing and multicore sampling is widely used. In sparse sensing, the support of a sampled signal is found by two most popular algorithms that compute sparse signal representations: matching pursuit (MP) [38, 51] and basis pursuit (BP) [11, 12]. In MP, a signal representation is iteratively and greedily found by choosing the atom that maximally improves the representation. On the other hand, BP seeks a representation that minimizes the L-1 norm of the coefficients. Once the support of the signal is found, the signal is recovered by a multicore algorithm. Previously, multicore signal reconstruction algorithms were used only with the time-offset-based hardware that generates multicore sampling patterns by applying different time offsets to each channel [70] or with a random-modulated wideband receiver [10, 35, 42]. As these types of architecture requires a large number

of samplers and accurate delay circuits with fine resolution or wideband mixers, the multicoset sampling architectures were not widely used in testing and measurement field.

In our first research, we assume the spectral support of the input signal is known a priori (or found by sparse sensing methods) and focus on the use of a multicoset-based signal reconstruction algorithm. To alleviate the practical concerns and cost of the conventional multicoset sampling, we propose a dual-rate sampling hardware system consisting of only two sampling modules to implement non-equispaced sampling. The use of a dual-rate sampler alleviates concerns about additional sampling noise that may be introduced by hardware non-idealities or configuration mismatches among multiple samplers, which in turn compromises the signal integrity of signal acquisition systems.

In practice, mismatches of the TIADCs cause undesired spectral components. The conventional mismatches are the offset, sample-time, and bandwidth mismatches. Many works have been researched to calibrate and compensate the mismatches [19, 63]. However, these calibration/compensation techniques are applied in the conventional single rate TIADCs. The first topic of this research also examines the methods to compensate the mismatched samples from two different sampling rates and empirically proves that the compensation improves the reconstruction quality.

2.2 Jitter Tracking and Eye-diagram Reconstruction by Incoherent Subsampling

Nonreal-time, or equivalent-time, jitter analyzers (or oscilloscopes) are another type of test instruments compared to the real-time sampling systems which was discussed in the previous section. A nonreal-time jitter analyzer is able to acquire high-speed signals with a much slower sampling rate than the Nyquist rate. For digital serial data testing, nonreal-time jitter analyzers use coherent subsampling instruments. These are further classified into random and sequential equivalent-time sampling schemes,

which are commonly used to acquire high-speed signals for jitter testing. It is because those schemes sample points over many repetitions of the input periodic signal, which can be used to analyze the statistics of the jitter in the input signal. However, the effective sampling rate can be increased only if the coherent subsampling method is provided by the extra RF/mixed signal circuitry. For example, the random equivalent-time sampling needs a time-to-digital converter (TDC) and an explicit trigger signal, and the sequential equivalent-time sampling requires a sequential time-delay generator. The sampling clock is sequentially delayed in order to sample a different time index over a period of the input signal (or a bit-period). In this type of oscilloscopes, the external clock trigger that is synchronized with the input signal and a precise delay circuitry is required. The additional timing subsystems complicate the overall systems of the nonreal-time jitter analyzers and their setups. Moreover, the measurement uncertainty and nonideality of the additional timing subsystems may limit the performance of the measurement. These technical difficulties may be overcome with various software-synchronization techniques which can be used in incoherent subsampling environment. In [4, 47, 50], the periodogram of the incoherently sample signal is used to estimate the discrete frequency (or period) of the input signal. Such a standard Fourier transform-base spectral analysis may be used only for online bit error rate monitoring that does not require very accurate synchronization. It may not be a proper method for the precise measurement that needs to be performed in the presence of noise, jitter and multiple aliased harmonic tones. In [30], the binary-tree data-truncation algorithm is used to reduce the computation time required to evaluate the periodogram of the input signal. This technique reduces computation burden and is beneficial for real-time synchronization. However, this approach alone may not be used for accurate measurement due to its inherent limitation of the frequency resolution.

To improve synchronization accuracy, [3, 5, 75] introduce a chirp z-transform

(CZT)-based software synchronization technique. The synchronization accuracy by this approach is found to be good enough unless the fundamental tone of the input signal contains high-frequency jitter or the aliased harmonics and distortions (due to subsampling) are placed near the fundamental tone. In this thesis, we evaluate the synchronization performance of the CZT-based approach and provide the comparison with our algorithm, especially in cases where the sampled signal is jittered and contains aliased distortions near the fundamental tone.

In [72, 73], another fine synchronization approach is proposed. This approach uses the statistical jitter quantity of the reconstructed eye-diagram as a cost function, so called a time-domain cost function. However, the time-domain jitter cost function requires a large sample size, especially on the rising/falling edges of the input signal, to generate a statistical jitter quantity. Furthermore, this technique does not provide a smooth cost function over the required frequency sweep range unless a large number of samples are acquired.

In our work, we exploit a software-based nonreal-time signal acquisition technique to achieve high-precision jitter characterization of high-speed pseudo-random bit sequences (PRBSs) with a simpler hardware configuration. First, the proposed method uses subsampling to increase the effective sampling rate of ADCs. Like other nonreal-time sampling approaches, it avoids the shortcoming of real-time sampling oscilloscopes requiring a fast sampling rate enough to capture the input bit sequences. Second, the proposed method uses incoherent sampling to avoid the complex timing circuitry that a coherent sampling device requires for synchronization. Third, we employ algorithmic clock recovery (CR) instead of using hardware CR subsystems. The proposed algorithmic CR approach differs from other algorithmic CR or software-synchronization techniques such as [50, 72] in the following ways:

- The accuracy of the proposed algorithmic CR is enhanced using the spectral interpolation (coarse estimation) and the selective discrete Fourier transform

(DFT) frames (fine estimation). The synchronization accuracy of this method (without using the fine-tuning) is comparable with or similar to the CZT-based method shown in [3, 75]. However, the proposed method reduces the computational burden by sequentially narrowing the frequency range of the spectral evaluation through multiple analysis steps.

- In the fine tuning process, a spectral jitter cost function is used to improve the frequency estimation and computational reliability, especially when the sampled signal contains jitter, aliased harmonics and distortions near the fundamental tone. The spectral jitter cost function exploits sparsity promotion in the frequency-domain, which is more stable than the time-domain cost function in [72, 73], especially when the sample size is small. Moreover, it performs significantly better when the signal is sampled with inherent jitter as compared to the CZT-based technique.

2.3 Eye-diagram monitoring and TDR with monobit receiver

The recent trend for faster devices and high-volume data storage increases demands on high-speed interconnections. The degradation of the high-speed signal, such as attenuation, ringing, reflection and crosstalk, is now important issues. According to [2], it is reported that the reasons for majority of the signal degradation are high-speed interconnects.

To mitigate the high-speed signal degradation and intersymbol interference (ISI), various equalization techniques have been considered. In the receiver front-end, continuous-time linear equalizers (CTLE) and decision feedback equalizers are commonly employed to compensate for the signal distortions and loss. Tuning the filter coefficients and implementing adaptive sampling in the receiver can be achieved because the channel information is captured by the samples. However, tuning the

equalization in the transmitter is not straightforward unless an extra physical link conveys the channel information from the receiver. In [74], the optimal equalizer coefficients of transmitter is obtained through a physical feedback line by handshaking with an adaptation logic in receiver. In [34] and [54], the strength of pre-emphasis is determined by estimating the channel length. In Figure 6(a), the channel length

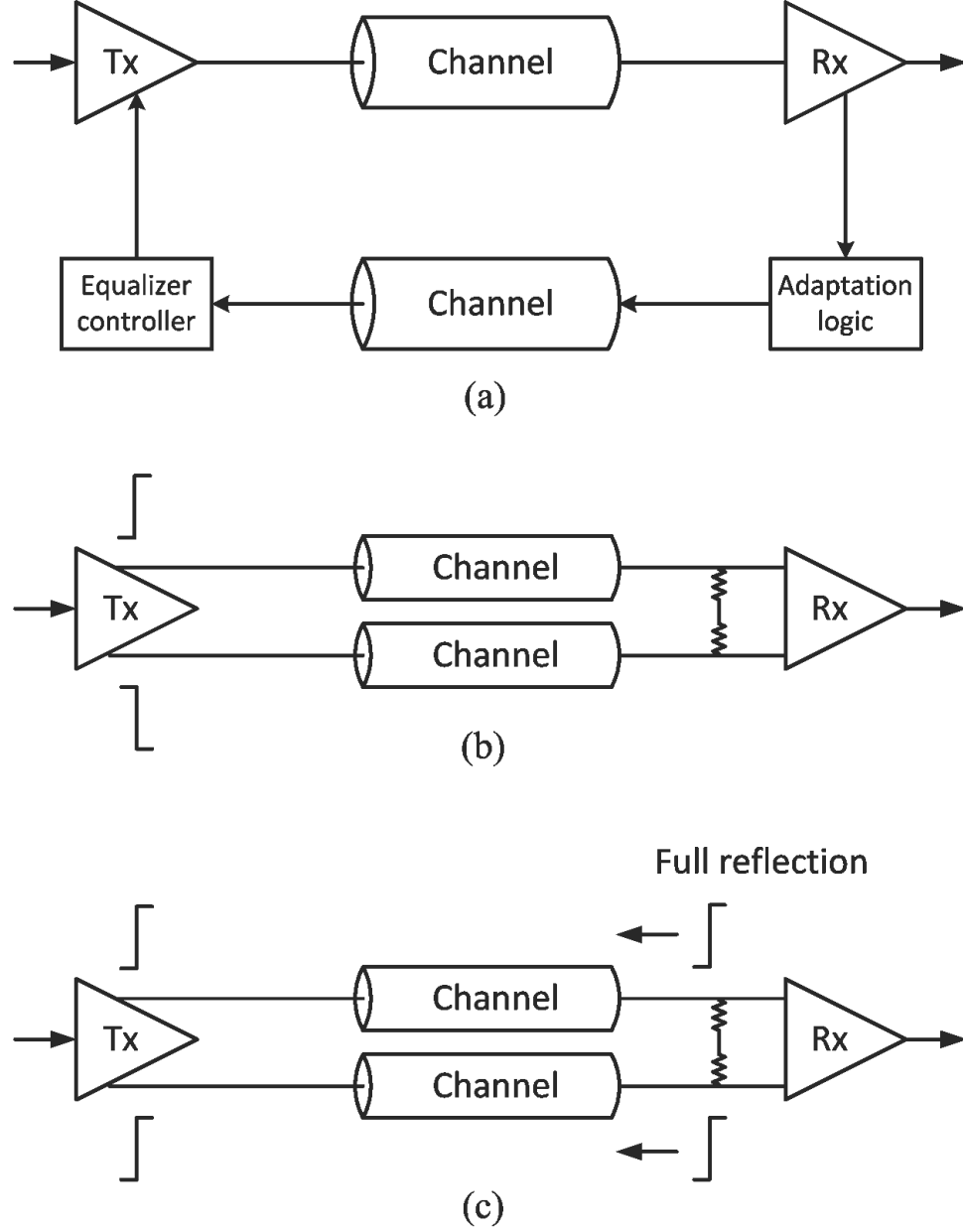


Figure 6: (a) Channel information is feedback by an extra line. (b) Normal mode signaling and (c) pre-emphasis calibration mode proposed in [54].

is calculated by the time of flight measured by an extra physical line forming a loop in [34]. An adaptive pre-emphasis calibration scheme based on the time-domain reflectometry (TDR) is proposed in [54]. In the normal signaling mode (Figure 6(b)), differential signals are transmitted resulting in no reflection when the resistance at the far-end forms a current path. In the calibration mode (Figure 6(b)), the differential lines become two single-ended links. As two identical signals reach at the far-end, no current flows through the resistor, which results in a full reflection. These works, however, consider only the channel length for the signal degradation.

Various researches to detect wiring/transmission line faults have been studied. In [54, 59], joint time-frequency domain reflectometry (TFDR) technique to detect multiple faults accurately is proposed. However, these works require a high-speed arbitrary waveform generator (AWG) to generate a chirp signal and a wideband circulator to isolate the reflected signal from the fault. In [58], spread spectrum time domain reflectometry (SSTDR) and sequence time domain reflectometry (STDR) are proposed. A spread spectrum signal is injected onto the wires and the observed reflected signal is correlated with a copy of the injected signal to detect the faults. This approach, however, demands a pair of duplicated pseudo-noise digital sequence generators and a correlator which is composed of a wideband mixer and an integrator circuit. Therefore, these approaches are not adequate and cost-efficient for diagnosing faults in digital high-speed interconnection due to extra signal generators and special circuitry.

In addition, eye-diagrams are used for evaluating the quality of high-speed digital signals [15]. Eye-diagrams of digital signals are constructed by remapping the samples over the bit-period so that the previous waveforms remain on the bit-period while subsequent ones are overlapped. In [23, 27], the analyses on eye-diagrams of digital signals are studied. They proposed stable and robust statistics which can derive various performance metrics such as root-mean-square jitter, eye-height, and eye-width. In

the recent work, eye-opening monitor (EOM) circuits are developed in on-chip level [49, 55]. In these works, the eye of the input data signal is measured by the recovered clock by CDR and the phase-shifted clock from the recovered one.

In this work, the proposed test architecture uses field programmable gate arrays (FPGAs) for pattern synthesis and sample acquisition. The FPGA logic is complemented by customized pin electronics (PE) modules including high-speed drivers and comparators. As FPGAs are capable of multi-channel IOs and the PE modules are constructed using off-the-shelf components, the cost of the test module is minimized as well as the multi-channel high-speed testing is achieved. Moreover, a novel algorithm that reconstructs a full TDR waveform without extra timing circuitry and a new approach diagnosing multiple faults in the channel achieves a robust channel monitoring while minimizing hardware cost. The contribution of this work can be summarized as:

- A new monobit test architecture and a dedicated reconstruction algorithm reduce the testing cost compared to the conventional approaches.
- Multiple faults can be detected and diagnosed by our impedance reconstruction algorithm.
- By the proposed approach, the high-speed transmitter is able to be tuned without communicating with the receiver.

CHAPTER III

WIDEBAND SIGNAL ACQUISITION BY DUAL-RATE TIME-INTERLEAVED UNDERSAMPLING HARDWARE AND MULTICOSET SIGNAL RECONSTRUCTION ALGORITHM

3.1 Proposed Approach

An overview of the proposed signal acquisition technique utilizing dual-rate (or two-channel) time-interleaved undersampling hardware and associated multicoset signal reconstruction algorithms is shown in Figure 7. The input test signal is simultaneously, but with different sampling frequencies (f_1, f_2), digitized by two wideband analog-to-digital converters (ADCs) clocked by two individual programmable sampling time-base generators that share a frequency reference oscillator. The two sets of discrete samples obtained from the two uniform samplers are transferred to a digital signal processor (DSP), where they are merged into a single sample set whose sample grid becomes nonuniform. The merged dual-rate samples are digitally classified into p sampling channels, where each sampling channel represents a uniform sample grid with a common sample interval, which is known as a multicoset. Based on the p sets of samples and a *priori* frequency band information of the test signal, a multicoset based signal reconstruction algorithm can be used to solve the linear system of p data sets and recover the original test signal in the frequency-domain as well as in the time-domain with enhanced time/frequency resolution beyond the original hardware sampling rate.

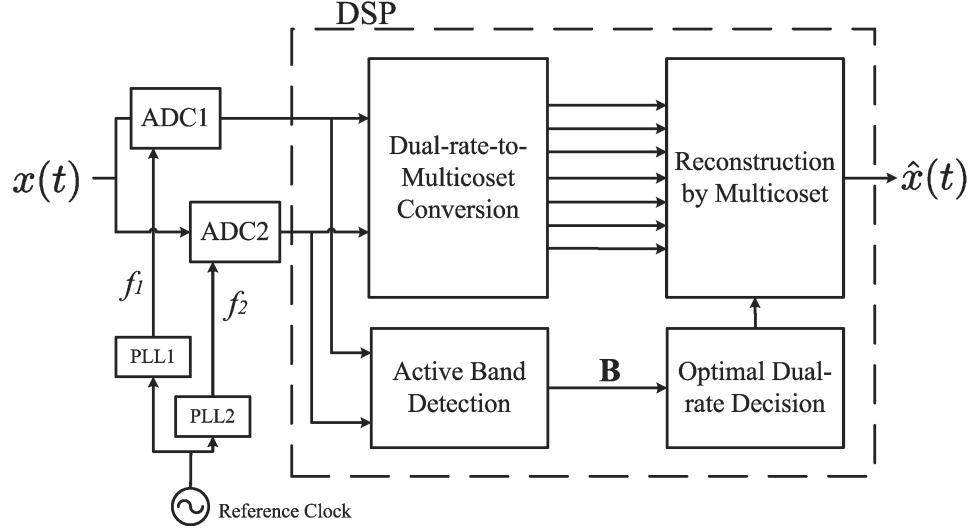


Figure 7: Block diagram of the proposed dual-rate time-interleaved undersampling and multicaset signal reconstruction.

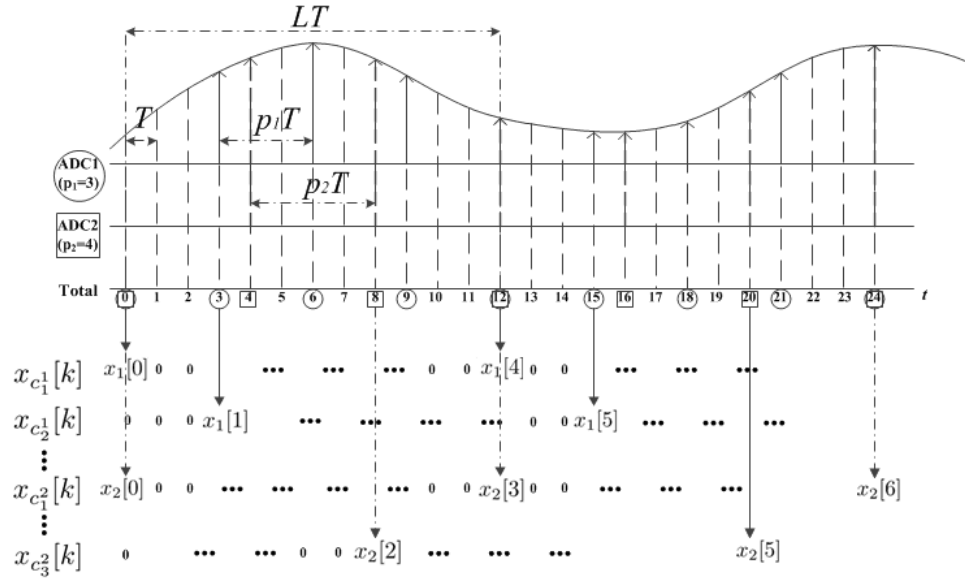


Figure 8: Samples from ADC₁ ($p_1 = 3$) and ADC₂ ($p_2 = 4$) are converted to multicaset sample sets on the uniform grid with a period $L = 12$.

3.1.1 Dual-rate Time-interleaved Undersampling

Let $x(t)$ be a continuous real signal defined over time t and let its continuous-time Fourier transform (CTFT) be

$$X(f) = \int_{-\infty}^{\infty} x(t) e^{-j2\pi ft} dt. \quad (3)$$

We assume that $x(t)$ is a band-limited, multiband signal with known frequency bands. The frequency bands of $x(t)$ are defined as

$$B = \pm \bigcup_{i=1}^n [a_i, b_i), \quad (4)$$

where $0 \leq a_1 < b_1 \dots < a_n < b_n$, which we call *active bands*.

It is well-known that a perfect reconstruction of the signal $x(t)$ is achieved by uniformly sampling a band-limited signal with a sampling frequency of $f_{\text{Nyquist}} = 2b_n$, where f_{Nyquist} is the Nyquist rate. In dual-rate time-interleaved undersampling, the signal $x(t)$ is sampled at two different sampling frequencies that are much lower than f_{Nyquist} . $x_1[k]$ and $x_2[k]$ are the discrete samples acquired by sampling the signal $x(t)$ with ADC₁ and ADC₂, whose sampling intervals are T_1 and T_2 respectively. In cases where both the acquired sample sets are phase aligned to a common reference time-base (assuming no relative phase errors), $x_1[k]$ and $x_2[k]$ are expressed as the following

$$\begin{cases} x_1[n] = x(nT_1), \\ x_2[n] = x(nT_2), \end{cases}, -\infty < n < \infty, \quad (5)$$

where the sampling intervals T_1 and T_2 are selected by using the equation shown below

$$\begin{aligned} T_1 &= p_1 T, \\ T_2 &= p_2 T, \end{aligned} \quad (6)$$

where p_1 and p_2 are *coprime* integers and T denotes the base sampling period (much smaller than T_1 and T_2) that can be *virtually* obtained via the proposed signal reconstruction technique. The discrete-time stamps of the two samplers are given by

$$C_1 = \{c_i^1 \mid c_i^1 = p_1 i : 0 \leq c_i^1 < L, i = 0, 1, \dots, p_2 - 1\}, \quad (7)$$

$$C_2 = \{c_i^2 \mid c_i^2 = p_2 i : 0 \leq c_i^2 < L, i = 0, 1, \dots, p_1 - 1\}, \quad (8)$$

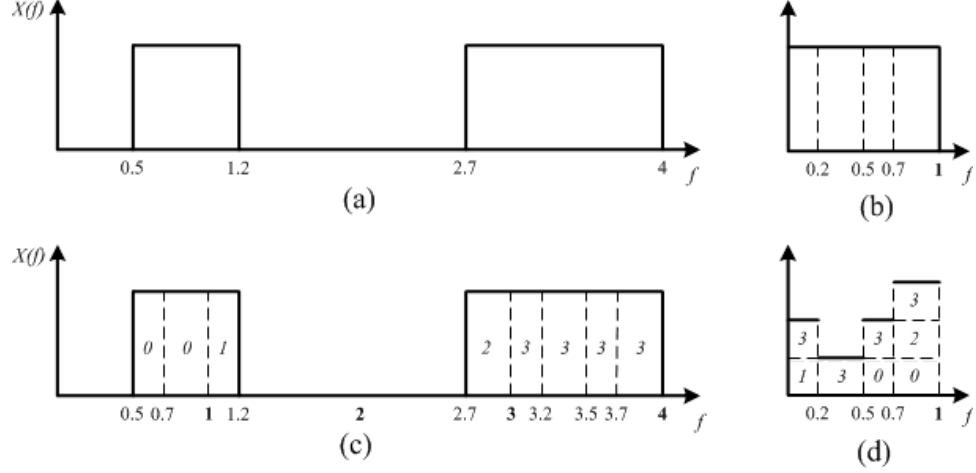


Figure 9: (a) Active bands of the test signal; (b) Aliased boundaries of active bands (G_m); (c) Active bands are divided into subintervals corresponding to G_m ; (d) Spectral index sets (k_m) and their cardinalities (q_m).

where L denotes the least common multiple (LCM) of the two co-prime integers p_1 and p_2 , which is $L = p_1 p_2$. A set of total discrete-time stamps containing both C_1 and C_2 is obtained by merging the two sets.

$$C_{\text{total}} = C_1 \cup C_2 = \{c_1, c_2, \dots, c_{p_{\text{total}}}\},$$

where p_{total} denotes the cardinality of C_{total} , which is $p_1 + p_2 - 1$.

In Figure 8, an example of the discrete-time stamps for dual-rate sample sets with $p_1 = 3$ and $p_2 = 4$ is illustrated, where a pattern of particular discrete-time stamps repeats every $L (= 12)$ discrete-time stamps. In this example, $C_1 = \{0, 3, 6, 9\}$, $C_2 = \{0, 4, 8\}$, $C_{\text{total}} = \{0, 3, 4, 6, 8, 9\}$, and the discrete-time stamps in C_{total} are *nonuniform*. Note that the pattern of discrete-time stamps in C_{total} is uniquely defined by p_1 and p_2 , whose selection scheme is studied in Section 3.3.

3.1.2 Dual-rate-to-multicoset Sample Re-sequencing

Dual-rate sample sets obtained from two distinct sampling rates are digitally converted to multicoset sample sets $(x_{c_i^1}, x_{c_i^2})$ by re-sequencing the raw samples as shown

below

$$x_{c_i^1}[k] = \begin{cases} x_1[lp_2 + i - 1] & , \text{if } k = lL + c_i^1, l \in \mathbb{Z}, \\ 0 & , \text{otherwise,} \end{cases} \quad (9)$$

$$x_{c_i^2}[k] = \begin{cases} x_2[lp_1 + i - 1] & , \text{if } k = lL + c_i^2, l \in \mathbb{Z}, \\ 0 & , \text{otherwise,} \end{cases} \quad (10)$$

where $k = 0, 1, 2, \dots, Ln - 1$. The number of samples in each coset is the same as the number of samples that can be virtually obtained from the base frequency $1/T$ because of zero-padding. Given L and p , the total number of possible cosets is $\frac{L!}{p!(L-p)!} = \binom{L}{p}$. The cyclic distance between the sample points determines the uniqueness of the cosets.

3.1.3 Multicoset Signal Reconstruction Algorithm

In this section, we provide a review of multicoset signal reconstruction algorithms [65, 66], which are used for signal reconstruction of the re-sequenced sample cosets provided in Section 3.1.2. In multicoset signal reconstruction, we choose subsamples from the samples of the base frequency, $1/T$. The subsamples are chosen to have a periodic pattern but do not necessarily have a uniform space between them. Then, we can define the sampling locations $(kL + c_i)T$ for any integer k , where L is the period of the sampling pattern, and c_i is a positive integer, and $0 \leq c_i < L$ for $i = 1, \dots, p$. We call the set $C = \{c_1, \dots, c_p\}$ the “cosets”.

For a given coset, c_i , the discrete-time sequence that samples the input signal at $(kL + c_i)T$ and zero-pads at the other points is described as

$$x_{c_i}[n] = \begin{cases} x(nT), & n = kL + c_i, \text{ where } k \in \mathbb{Z}, \\ 0 & , \text{otherwise.} \end{cases} \quad (11)$$

The discrete-time Fourier transform (DTFT) of the sequence x_{c_i} is expressed as

$$Y_{c_i}(e^{-j2\pi fT}) = \frac{1}{LT} \sum_{r=0}^{L-1} X\left(f + \frac{r}{LT}\right) e^{\frac{j2\pi r c_i}{L}}, \quad f \in F_0, \quad (12)$$

where $F_0 = [0, \frac{1}{LT})$ and $X(f)$ is the CTFT of $x(t)$ as defined in (3)¹. The right-hand side of (12) describes the spectral aliasing due to the undersampling by L (the summation of the CTFT L times) and the phase-shift due to the time-offset of c_i (the complex exponential at the end of the equation). Note that the sequence x_{c_i} is composed of the c_i discrete-time delayed samples downsampled by a factor of L with $L - 1$ interleaved zeros.

Now, we consider the aliased boundaries of the active bandwidth (4) defined by the following

$$\Gamma = \bigcup_{i=1}^n \text{mod}(a_i, \frac{1}{LT}) \cup \bigcup_{i=1}^n \text{mod}(b_i, \frac{1}{LT}) \cup \{0, \frac{1}{LT}\}, \quad (13)$$

where a_i and b_i are defined as the lower and upper bound of the i -th frequency band in (4).

Let the increasing-order elements of the set Γ be $\{\lambda_0 = 0, \lambda_1, \dots, \lambda_M = \frac{1}{LT}\}$, and then the frequency interval of the aliased boundaries can be defined as

$$G_m = [\lambda_{m-1}, \lambda_m), \quad 1 \leq m \leq M - 1. \quad (14)$$

Note that the frequency domain of X_{c_i} , F_0 , is divided into M number of subintervals.

For each subinterval, define the “spectral index sets” as

$$k_m = \{r | X\left(f + \frac{r}{LT}\right) \subset F, f \in G_m\},$$

and their cardinality (the number of element of a set) as $q_m \leq L$. Let $k_m(l)$ denote the l -th element of k_m if k_m is not empty. The spectral index sets indicate which part of the active bandwidth contributes X_{c_i} .

¹The Fourier transforms discussed in this section are CTFT and DTFT. Therefore, the variable f is a continuous variable. Note that the variable f is an unbounded real number in (3), whereas f in (12) is a bounded real number of the bounded set F_0 .

By the definition of the spectral index sets, (12) is reduced as follows

$$Y_{c_i}(e^{-j2\pi fT}) = \frac{1}{LT}X\left(f + \frac{k_m(1)}{LT}\right)e^{\frac{j2\pi k_m(1)c_i}{L}} + \dots \\ + X\left(f + \frac{k_m(q_m)}{LT}\right)e^{\frac{j2\pi k_m(q_m)c_i}{L}}, f \in G_m,$$

where the RHS is the summation of the $q_m \leq L$ terms, while (12) is that of L terms.

Example: Suppose the input signal bandwidth is given as $B = [0.5, 1.2) \cup [2.7, 4)$ (Figure 9(a)). Let $L = 12$ and $T = 1/12$. By (13), we obtain $\Gamma = \{0, 0.2, 0.5, 0.7, 1\}$ and $M = 4$ (Figure 9(b)). The frequency intervals of Γ in (14) are

$$G_0 = [0, 0.2), \quad G_1 = [0.2, 0.5), \\ G_2 = [0.5, 0.7), \quad G_3 = [0.7, 1).$$

The spectral index sets and their cardinalities are the following (Figure 9(d)):

$$k_0 = \{1, 3\}, \quad q_0 = 2; \\ k_1 = \{3\}, \quad q_1 = 1; \\ k_2 = \{0, 3\}, \quad q_2 = 2; \\ k_3 = \{0, 2, 3\}, \quad q_3 = 3.$$

In summary, (12) is expressed in matrix form as follows

$$\mathbf{y}(f) = \mathbf{A}_m \mathbf{x}_m(f), \quad f \in G_m, 1 \leq m \leq M, \quad (15)$$

where $\mathbf{y}(f)$ is a p -length vector, $\mathbf{x}_m(f)$ is a q_m -length vector and \mathbf{A}_m is a p -by- q_m matrix. They are defined as follows:

$$[\mathbf{y}(f)]_i = Y_{c_i}(e^{-j2\pi fT}), \quad i = 1, \dots, p, \quad f \in G_m; \\ [\mathbf{x}_m(f)]_k = X\left(f + \frac{k_m(k)}{LT}\right), \quad k = 1, \dots, q_m, \quad f \in G_m; \\ [\mathbf{A}_m]_{ik} = \frac{1}{LT}e^{\frac{j2\pi c_i k_m(k)}{L}}. \quad (16)$$

Each element of the vectors $\mathbf{y}(f)$ and $\mathbf{x}_m(f)$ is a function of a continuous variable $f \in G_m$. Equation (15) can be easily understood by fixing f as any number in G_m . Then, the equation becomes a typical p -by- q_m linear system. In the next section, f is discretized by the Discrete Fourier Transform (DFT). Therefore, f will become a finite-dimension vector and for each element its corresponding linear system will be created.²The reconstruction of the original signal is achieved by solving (15) for each m . Depending on the dimensions of \mathbf{y} and \mathbf{x}_m and the rank of \mathbf{A}_m , the uniqueness and the existence of the solutions are determined. In general, if $p \geq q_m$ and \mathbf{A}_m is a full column rank matrix, the system is overdetermined, and thus we can apply the Moore-Penrose pseudoinverse to compute a least-square solution to the system.

²The equations for the linear system will not be explicitly described here because they are exactly the same as (15) and (16) except f is converted to a discrete variable by DFT.

3.2 *Active Band Detection*

In the previous section, the active bands are the *a priori* information for the reconstruction algorithm. For a signal with arbitrary active bands, however, the detection of the active bands is required for the full reconstruction. In this section, the active band sensing algorithm based on the Orthogonal Matching Pursuit (OMP) and asynchronous multirate sampling proposed in [64] is introduced.

The active bands are detected by comparing the aliasing spectra undersampled by two (or more) different sampling frequencies. The aliased spectra by each sampling frequency are unfolded and converted to analog frequencies. The sensing matrix, specially defined as the extended version of the Discrete Fourier Transform (DFT) matrix, projects the undersampled time-domain samples onto a common frequency basis. The common frequency basis is selected to align the two different DFT spectral grids. Once the aliased spectra are compared by the sensing matrices, the frequency support containing the highest energy in both spectra is chosen to be the first detected active band. The detected spectral component is then subtracted from the original waveform. This entire process (conversion, detection and subtraction) is iterated until the energy of the residual waveform reaches the stopping criteria.

The success rate for the detection increases with the number of different sampling rates. Because the algorithm can use asynchronous sample sets, two or more sample sets can be captured ahead of the dual-rated multicoset algorithm to provide more precise band locations.

3.3 *Dual-rate Sampling Frequency Optimization*

Given that the active bands of the test signal are known *a priori*, the optimal combination of the dual sampling rates can be found. In the proposed approach, f_1 is set to the maximum sampling rate (1.2-Gsps) that our custom hardware module can

achieve, and f_2 is tuned with 10-MHz resolution to find the optimal sampling frequencies. The optimality of the sampling frequency configuration (for the test signal with particular active bands) is verified by measuring the normalized mean square error (NMSE) of the reconstructed signal. In addition, the performance of signal reconstruction of dual-rate sampling with the optimal sampling frequency configuration is compared to that of the conventional multicoset sampling hardware.

3.3.1 Base Frequency

The base sampling rate $1/T$ should be set higher than $f_{\text{Nyquist}} = 2b_n$ to obtain a perfect reconstruction without spectral aliasing. Equation (6) results in a necessary condition for f_b as follows.

$$f_b = \frac{1}{T_b} = p_1 f_1 = p_2 f_2 > f_{\text{Nyquist}}, \quad (17)$$

where $f_1 = 1/T_1$ and $f_2 = 1/T_2$. The base sampling frequency is represented in an exclusive form of f_1 and f_2

$$f_b = \frac{f_1 f_2}{\text{gcd}(f_1, f_2)} > f_{\text{Nyquist}}, \quad (18)$$

where $\text{gcd}(f_1, f_2)$ is the greatest common divisor of f_1 and f_2 . Suppose that f_1 and f_2 are any positive integers, and that p_1 and p_2 are coprime integers. If $f_1 p_1 = f_2 p_2$, then $p_1 = \frac{f_2}{\text{gcd}(f_1, f_2)}$ and $p_2 = \frac{f_1}{\text{gcd}(f_1, f_2)}$.

3.3.2 Number of Base Samples

The number of base samples N_b is defined as the number of samples in the reconstructed signal represented with the base frequency (or sampling rate) $f_b = 1/T_b$. As shown in Figure 8, N_b is equal to the number of samples in each re-sequenced coset including zero-padding. In the sampling case shown in (6), $p_2 n$ samples are obtained from ADC_1 and $p_1 n$ samples from ADC_2 . Therefore, the number of base samples is determined by

$$N_b = p_1 p_2 n = Ln, \quad (19)$$

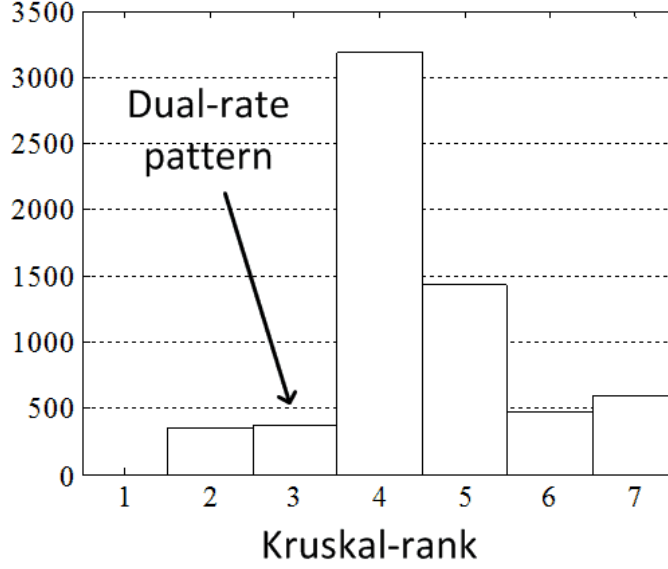


Figure 10: Kruskal-rank histogram of $L = 12$ and $p = 6$. The Kruskal-rank of the dual-rated pattern, $C = \{0, 3, 4, 6, 8, 9\}$, is 3.

and it is regulated with an upper bound. The upper bound constraint is required to efficiently use the memory and computational power of the digital signal processors (DSPs). As each coset occupies N_b , the total number of samples used in estimating a reconstructed signal is $N_b(p_1 + p_2 - 1)$. Note that $\mathbf{y}(f)$ and $\mathbf{x}_m(f)$ in (15) are represented by using the DTFT operation. However, when the algorithm is implemented in the DSP, the discrete Fourier transform (DFT) or fast Fourier transform (FFT) operation must be used. The DTFT of a coset sequence in (12) is approximated by the DFT of N_b samples per coset in the DSP. The total amount of computation required for the DFT operation of all the coset sequences is $(p_1 + p_2 - 1)O(N_b \cdot \log N_b)$.

3.3.3 Less Deficient Linear System

The reconstructed spectrum is obtained by solving the system equation (15) for \mathbf{x}_m . Note that \mathbf{A}_m is the conjugated submatrix of the L-by-L DFT matrix by extracting its rows indexed by the coset (C) and columns indexed by k_m . Though a DFT matrix is a full-rank matrix, its submatrix may not be full-rank.

A key property of sampling patterns that successfully reconstruct the original signal is the Kruskal-rank of the sampling matrix [32]. The Kruskal-rank of \mathbf{A} , $\sigma(A)$, is defined as the maximal number k such that every set of k columns of \mathbf{A} is linearly independent. A sampling pattern is called “universal” when the pattern has full Kruskal-rank, i.e., $\sigma(A) = p$. Therefore, a universal sampling pattern simplifies the condition of the uniqueness to $p \geq q_m$. We now address the question of how the dual-rated pattern is better or worse than the other patterns. As the number of possible patterns is usually very large, a simple case of $L = 12$ and $p = 6$ is chosen for instance. We generated all the possible patterns including the dual-rated pattern $C = \{0, 3, 4, 6, 8, 9\}$ and computed the Kruskal-rank of each pattern. The histogram of the Kruskal-rank is shown in Figure 10. The figure indicates that the dual-rated pattern may not achieve the universal pattern. Therefore, it is necessary to check the rank of the sampling matrix and verify if the matrix is full-rank.

Moreover, if the number of rows is less than the number of columns, the system is underdetermined, which means the number of solutions is infinite. Therefore, it is desired that the sampling matrix \mathbf{A}_m 1) is full-rank and 2) has more rows than columns. The second statement can be reduced to $p \geq \max_m q_m$. Note that q_m is the cardinality of the spectral index or the number of the overlapped active bandwidth in G_m . It is related to how “sparse” the input signal is. When the input signal is too “broad”, there is a higher chance that q_m is a large number. However, the sparsity of the input signal does not directly determine q_m . This is because q_m is determined by LT (the sampling rate of a coset, which decides the amount of spectral fold) as well as the active bandwidth. In this paper, the signal is assumed to be sufficiently sparse that p can outnumber q_m .

Because we assume the rows outnumber the columns, the sampling matrix is full column rank when $\text{rank}(\mathbf{A}_m) = q_m$. Note that the rows and columns of the sampling matrix, A_m , are determined by the sampling pattern (rows) and the spectral index

Table 1: INPUT TEST SIGNALS FOR NUMERICAL SIMULATION

| Band(GHz) | Mod Type | f_c (GHz) | rate | dev |
|--------------|------------|-------------|--------|--------|
| [0.25, 0.33] | AM | 0.29 | 39MHz | NA |
| | FM | 0.29 | 50kHz | 20MHz |
| | SSB(upper) | 0.315 | 5MHz | NA |
| [1.95, 2.15] | FM | 1.965 | 1MHz | 5MHz |
| | FM | 2.02 | 50kHz | 20MHz |
| | FM | 2.056 | 50kHz | 6MHz |
| | FM | 2.09 | 50kHz | 18MHz |
| | FM | 2.136 | 200kHz | 10MHz |
| [6.00, 6.15] | PM | 6.005 | 1MHz | 0.1rad |
| | FM | 6.043 | 1MHz | 1MHz |
| | PM | 6.09 | 10MHz | 0.3rad |
| | PM | 6.145 | 1MHz | 0.3rad |

(columns) in (16). Therefore, the rank of the sampling matrix can remain the same or decrease depending on the choice.

As the matrix size varies with the combination, it is not proper to evaluate the rank of the sampling matrix as the objective function. In this case, it is more convenient to see how far the rank of the matrix is from the full rank, i.e., the deficiency of the system. The deficiency of the overall system is defined as

$$D(f_1, f_2) = \sum_{m=1}^{m=M} [q_m - \text{rank}(\mathbf{A}_m)]. \quad (20)$$

When all M subsystems are full column rank, D is 0. Otherwise, the amount of deficiency is stacked over the subsystems. Therefore, we choose a combination of f_1 and f_2 that minimizes D .

3.3.4 Numerical Simulation

Via numerical simulation, we compare the reconstructed signal obtained from the optimal sampling with that from non-optimal sampling. The test signal consists of various modulated signals (amplitude modulated, frequency modulated and phase modulated) with different carrier frequencies. Table 1 summarizes the test signal

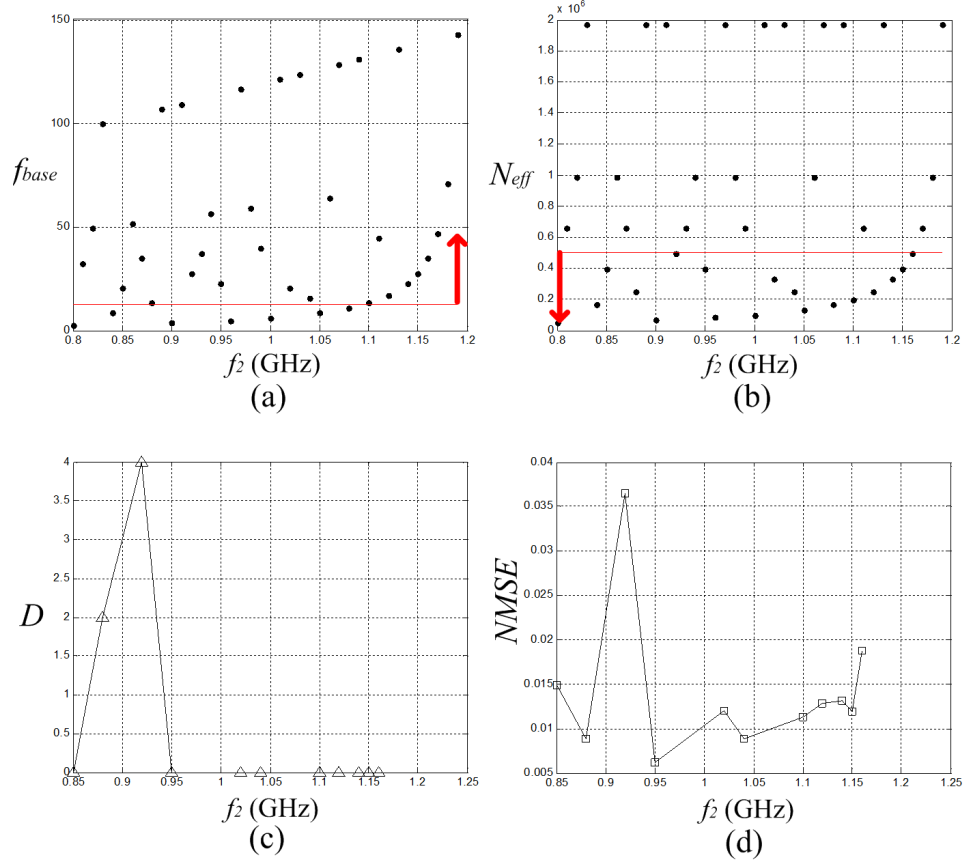


Figure 11: (a) The base frequency over f_2 . (b) The effective number of sampling over f_2 . (c) The objective function over f_2 . (d) The NMSE over f_2 .

specification. The test signal also includes Gaussian white noise. The first sampling frequency is fixed at 1.2GHz, which is the maximum sampling frequency of the hardware and the second sampling frequency is swept under 1.2GHz.

Before running the dual-rate multicoset algorithm, the asynchronous active band detection from Section 3.2 is performed. Three different sampling rates (1.2GHz, 1.15GHz, and 1.104GHz) and 1400 samples for each sample set are used to detect the active bands. As a result, three active bands are detected; [251MHz-329.1MHz], [1959.9MHz-2148.3MHz], and [6004.3MHz-6148.2MHz].

The base sampling rates corresponding to the second sampling rates are shown in Figure 11(a). The minimum sampling rate required to reconstruct the signal without aliasing is $f_{Nyquist} = 2b_n = 12.3$ GHz. The red horizontal line indicates the minimum

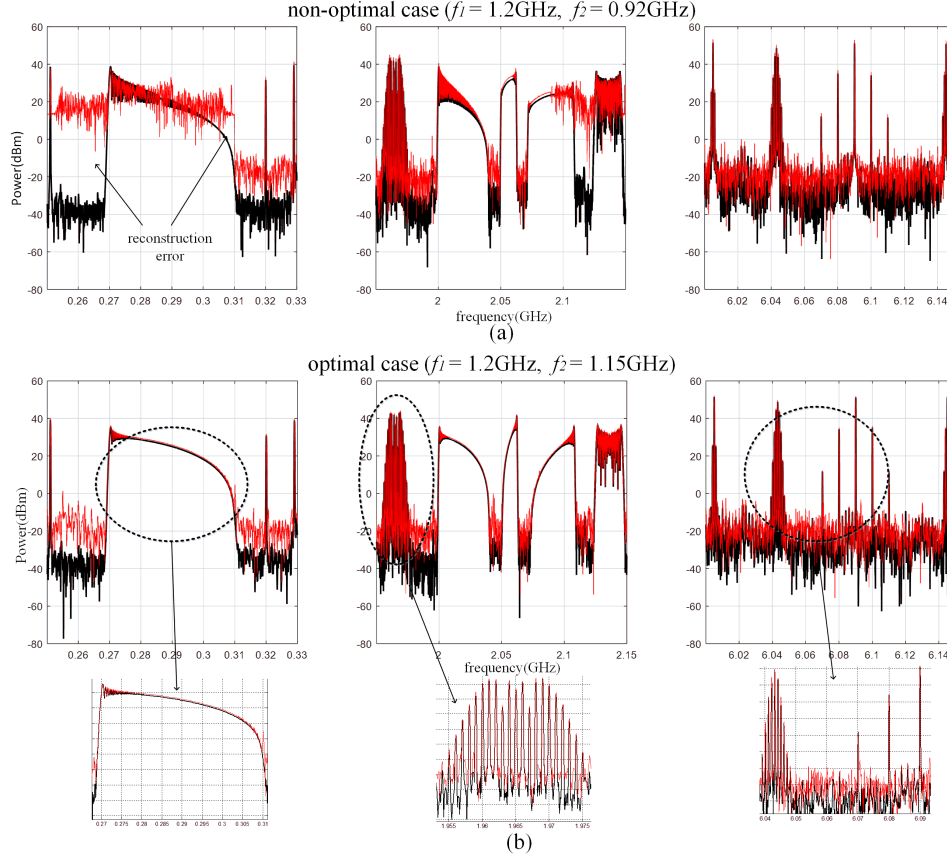


Figure 12: Comparison of the spectrum between the reconstructed signal and the original signal with a non-optimal and an optimal combination.

sampling rate. The effective numbers of samplings given that each ADC collects $16 \cdot 1024$ samples are shown in Figure 11(b). To conserve the memory and computational resources, the maximum effective number of samples is limited to $5 \cdot 10^5$. The red horizontal line indicates the maximum effective number of samples. The rank deficiency, $D(f_1, f_2)$, is plotted in Figure 11(c). This cost function can be calculated by the given active frequency bands of the input signal and the two sampling rates. Thus, the cost function can be obtained before reconstruction of the signal. The normalized mean-squared-error (NMSE) is shown in Figure 11(d). The NMSE is defined as the squared error between the DFT by the uniform sampling at the base frequency and the reconstructed DFT by the proposed algorithm.

In Figure 12, the reconstructed spectra by a non-optimal case ((a), $f_2 = 0.92\text{GHz}$,

$D = 4$) and an optimal case ((b), $f_2 = 1.15\text{GHz}$, $D = 0$) are compared. The reconstructed spectrum (red) and the original spectrum by uniform sampling at the base frequency (black) are plotted to visualize the amount of reconstruction error. It is notable that significant reconstruction errors are presented in the non-optimal case. In contrast, the reconstructed spectrum in the optimal case matches well with the original spectrum. In both cases, the noise floor is increased by the noise component outside the active bandwidth.

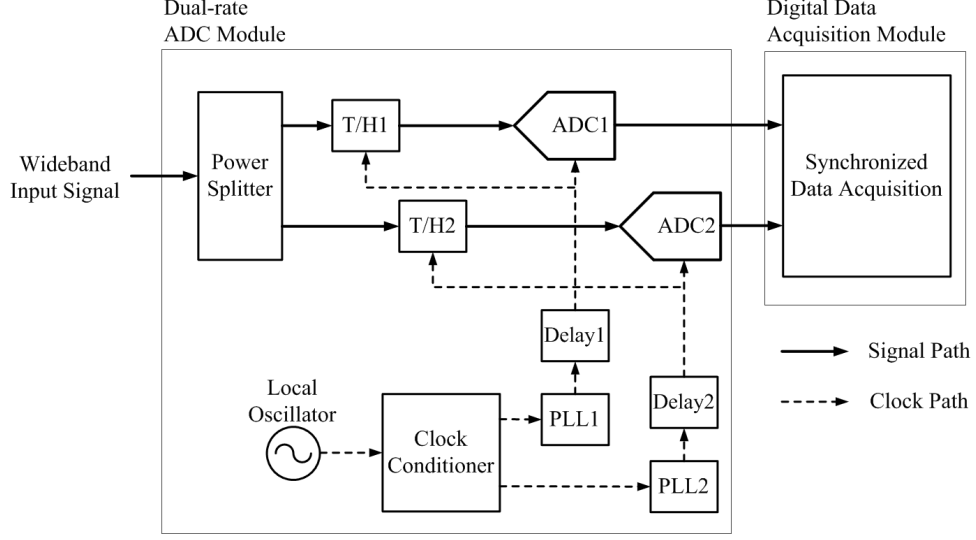


Figure 13: Block diagram of the proposed dual-rate time-interleaved undersampling hardware consisting of two hardware modules: the dual-rate ADC module and the digital data acquisition module.

3.4 *Hardware Validation: Dual-rate Time-interleaved Undersampling*

The proposed dual-rate time-interleaved undersampling scheme was implemented in two hardware modules: a dual-rate analog-to-digital converter (ADC) module and a digital data acquisition module, as shown in the block diagram in Figure 13. The dual-rate ADC module acquires the input analog signal at dual sampling rates to generate nonequispaced digital samples. The obtained digital sample data are transferred through high-speed multi-pin connectors to the digital data acquisition module, which stores the sample data in memory for digital post-processing that is performed offline.

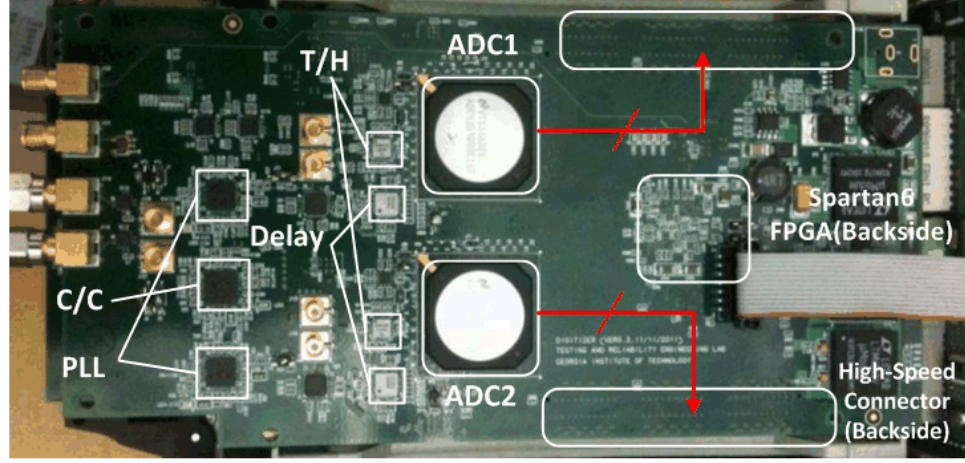
In Figure 13, the signal acquisition paths are denoted by solid lines. The input analog signal is divided in power by a wideband power splitter. The divided signals are individually fed to wideband track-and-hold (T/H) amplifiers. These T/H amplifiers are used as an analog front-end of the dual-rate ADC module and help increase the overall analog bandwidth beyond the given input bandwidth of the ADCs being used (ADC12D1800, Texas Instruments) by sampling/holding the signal at the front-end

with minimal signal distortion. The high-speed 12-bit ADCs are able to operate with a sampling clock with a frequency of up to 1.8-GHz and to cover a 3-GHz input bandwidth (when the T/H amplifier is not used as an analog front-end). The ADCs acquire the signal in the hold mode at the output of the T/H amplifiers.

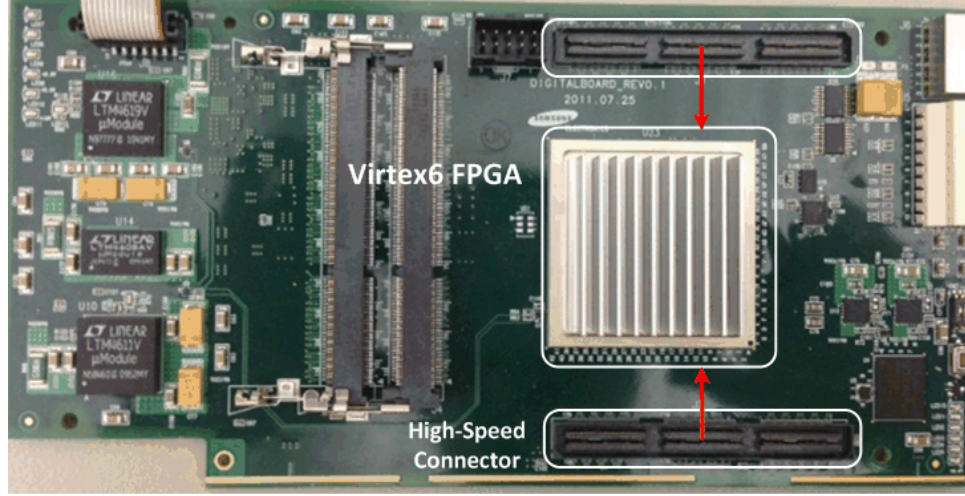
We choose two different models of the T/H amplifier with different input bandwidths on purpose to create gain/phase mismatch between the divided signal paths as shown in Figure 13. The T/H amplifier used for the upper channel (HMC5641BLC4B, Hittite) has 5-GHz of bandwidth, and the T/H amplifier for the lower channel (HMC5640BLC4B, Hittite) has 18-GHz of bandwidth. A compensation technique for gain/phase mismatch is described in Section 3.4.2. The digitized samples obtained by the combination of T/H amplifiers and ADCs are collected by a field-programmable gate array (FPGA) mounted on the digital data acquisition module.

The sampling time-base (or clock) paths are denoted by dashed lines in Figure 13. A 100-MHz crystal oscillator is used as a common frequency source for the sampling time-base of the ADCs as well as the system clock of the onboard FPGA (Spartan 6, Xilinx). To alleviate concerns regarding jitter noise of the reference oscillator, which might increase the sampling noise of the ADCs, we use a clock conditioner (LMK040033BISQ, National Semiconductor) to reduce the unwanted jitter component of the reference oscillator. Based on the reference frequency of the conditioned clock source, two programmable frequency synthesizers (LMX2541SQ3320E, National Semiconductor) generate high-frequency sampling time-bases for the two ADCs. Before being provided to the ADCs, the sampling clock signals are time-delayed by dedicated delay components (HMC856LC5, Hittite), which are used to control the relative delay of the two sampling clocks (Details of the use of the delay components are discussed in Section 3.4.1).

The onboard FPGA controls and programs these mixed-signal components in the dual-rate ADC module. Pictures of the dual-rate ADC module and the digital data



(a)



(b)

Figure 14: (a) Picture of the dual-rate ADC module. (b) Picture of the digital data acquisition module.

acquisition module are shown in Figure 14.

3.4.1 Sampling Phase Synchronization

The dual-rate-to-multicoset sample re-sequencing described in Section 3.1.2 assumes no relative sampling phase offset between the initial sampling phases of the dual-rate sample sets. In such an ideal case, the initial sampling phases of the two data sets should be aligned in exactly the same phase. However, in practice, the amount of phase offset varies depending on the arrival time of the trigger signal initiating data

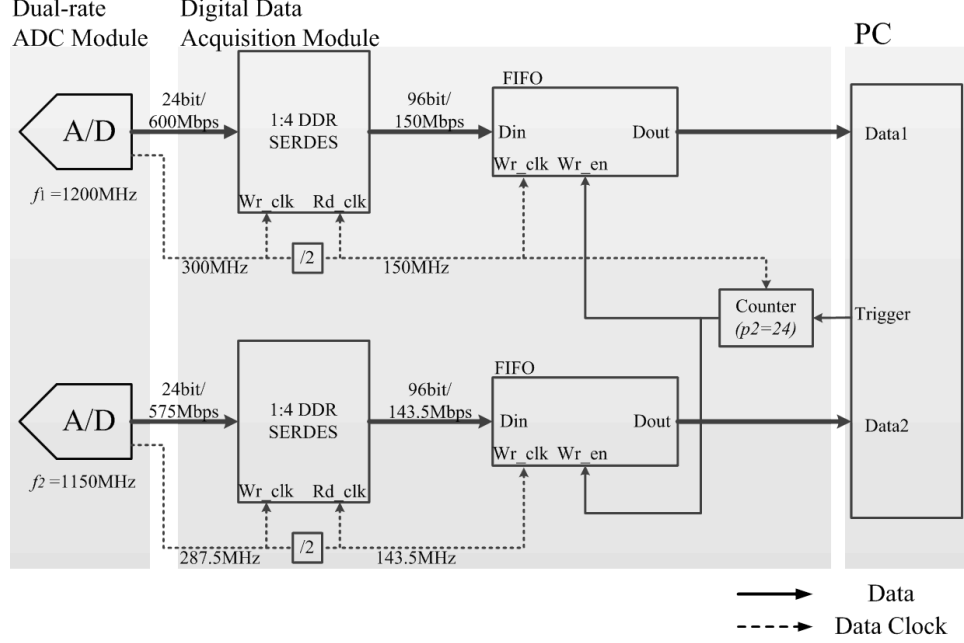


Figure 15: FPGA logic diagram of the digital data acquisition module.

acquisition. This random phase offset occurs due to the asynchronous trigger time with the dual-rate sampling frequency.

We propose an empirical method for phase-synchronizing dual-rate sample data sets. A potential phase offset (due to a potential timing mismatch between either the signal acquisition paths or the sampling time-base paths) between two sets of the obtained signal samples with different sampling rates is not constant over the data acquisition period. Due to this fact, the phase alignment of the two sample sets is not a simple task.

In the digital data acquisition module, the digital sample sets transferred from the dual-rate ADC module are deserialized and fed to FIFO logics implemented in the FPGA. To prevent uncertainty in the amount of phase offset, we implemented a synchronization logic associated with the FIFOs and deserializers. Using the fact that the relative phase between the two clocks is periodic with every p_2 of the first clock (or every p_1 of the second clock), the trigger signal is synchronized with an edge-detecting counter of the first clock. This trigger mechanism forces the write-enable

of the FIFO to be issued on a certain phase relationship. The FPGA logic diagram is shown in Figure 15, where $f_1=1.2$ -GHz and $f_2=1.15$ -GHz. The ADC12D1800 outputs the data at half the sampling rate on twice the number of buses. The output data are deserialized by 1-to-4 DDR SERDES of Virtex6 in the digital data acquisition module. Then, the deserialized data are stored in the FIFO. Therefore, the phase offset between the two data sets is determined by the write-enable of the FIFO. Note that the trigger signal is synchronized with one of the sampling clocks. The counter holds the trigger signal until the current state is equal to p_2 .

3.4.2 Calibration - Mismatch Compensation

Gain/phase mismatch between the two data acquisition channels (including T/H amplifiers and ADCs) is not negligible in cases where wideband signal acquisition is performed. Associated signal distortion needs to be compensated for prior to the signal reconstruction. The types of mismatch we consider are frequency-dependent gain and phase mismatches. These mismatches potentially result from channel delay skew and chip-to-chip performance variation of ADCs and T/H amplifiers. In this section, the second signal acquisition channel is considered a reference channel for simplicity. The channel mismatch, $F(f)$, is defined as

$$X_1(f) = F(f)X_2(f), \quad (21)$$

where $X_1(f)$ and $X_2(f)$ are the continuous Fourier Transform of the input signal of ADC₁ and ADC₂ respectively, and $F(f)$ is the frequency response of the first signal acquisition channel when the second channel is assumed ideal.

The mismatch compensation terms are applied to (15), and $m = 1$ is assumed for simplicity. The diagonal element $F_i = |F_i|e^{j\phi_i}$ represents the approximated piecewise gain ($|F_i|$) and phase (ϕ_i) mismatch of $F(f)$ where $\frac{k(i)}{LT} \leq f < \frac{k(i)+1}{LT}$. Note that the rank of the new system matrix AQ remains the same because Q is full column rank. Therefore, as long as the original system matrix A is of full column rank, the

$$\begin{aligned}
\underbrace{\begin{bmatrix} Y_{c_0^1} \\ \vdots \\ Y_{c_{p_2-1}^1} \\ Y_{c_0^2} \\ \vdots \\ Y_{c_{p_1-1}^2} \end{bmatrix}}_{\mathbf{y}(f)} &= \frac{1}{LT} \cdot \underbrace{\begin{bmatrix} e^{j2\pi c_0^1 k(1)} & e^{j2\pi c_0^1 k(2)} & \dots & e^{j2\pi c_0^1 k(q)} \\ \vdots & \vdots & \ddots & \vdots \\ e^{j2\pi c_{p_2-1}^1 k(1)} & e^{j2\pi c_{p_2-1}^1 k(2)} & \dots & e^{j2\pi c_{p_2-1}^1 k(q)} \\ e^{j2\pi c_0^2 k(1)} & e^{j2\pi c_0^2 k(2)} & \dots & e^{j2\pi c_0^2 k(q)} \\ \vdots & \vdots & \ddots & \vdots \\ e^{j2\pi c_{p_1-1}^2 k(1)} & e^{j2\pi c_{p_1-1}^2 k(2)} & \dots & e^{j2\pi c_{p_1-1}^2 k(q)} \end{bmatrix}}_{\mathbf{A}} \\
&\cdot \underbrace{\begin{bmatrix} F_1 & \dots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \dots & F_q \\ 1 & \dots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \dots & 1 \end{bmatrix}}_{\mathbf{Q}} \cdot \underbrace{\begin{bmatrix} X(f + \frac{k(1)}{LT}) \\ X(f + \frac{k(2)}{LT}) \\ \vdots \\ X(f + \frac{k(q)}{LT}) \end{bmatrix}}_{\mathbf{x}(f)}, \quad f \in G. \tag{22}
\end{aligned}$$

least-square solution of \mathbf{x} is still achieved by the pseudo-inverse of AQ . Equation (15) can be separated into two channels as shown in (22).

The mismatch matrix F can be found by applying a known single-tone test signal to the two signal acquisition channels and measuring the gain and phase offset between the channels in the digital signal post-processing. As the input signal and the sampling clock are not synchronized, the spectral leakage prevents an accurate estimation. A fractional DFT basis is used to estimate the fundamental frequency of the input signal. This method is used to fold back the samples over the fundamental period of the input signal, and then the non-equispaced DFT is performed to evaluate the gain and phase for the samples from each ADC.

The non-equispaced DFT basis for the fundamental frequency can be defined as

$$\begin{aligned}
\mathbf{v} \equiv \frac{1}{\sqrt{N}} [& e^{-j2\pi t_d[0]/N} \ e^{-j2\pi t_d[1]/N} \ e^{-j2\pi t_d[2]/N} \\ & \dots \ e^{-j2\pi t_d[N-1]/N}]^T, \tag{23}
\end{aligned}$$

where $t_d[k]$ is the time-location of the $(k-1)$ th sample. Then, the gain mismatch

and the phase mismatch in $[\frac{k(i)}{LT}, \frac{k(i)+1}{LT}]$ is described as

$$|F_i| = \frac{|\mathbf{v} \cdot \mathbf{x}_1|}{|\mathbf{v} \cdot \mathbf{x}_2|}, \quad (24)$$

$$\phi_i = \arg(\mathbf{v} \cdot \mathbf{x}_1) - \arg(\mathbf{v} \cdot \mathbf{x}_2), \quad (25)$$

where \mathbf{x}_1 and \mathbf{x}_2 are the samples from ADC1 and ADC2 for the corresponding sub-band.

The reasonable frequency for the single-tone test signal will be at half of its range, $f_m = \frac{k(i)}{LT} + \frac{1}{2LT}$. However, the simple frequency relationship between the test signal (f_t) and the sampling clock (f_s) does not generate fine resolution for $t_d[k]$. For example, if $f_t = \frac{f_s}{3}$, the time sequence $t_d[k]$ will be clustered into only three sample points, which is not sufficient to evaluate the gain and phase of the input signal. In other words, if the test signal and the sampling clock are related by

$$f_t = \frac{N}{M} f_s, \quad (26)$$

where N and M are coprime integers, then the time sequence $t_d[k]$ is clustered into M number of sets. Therefore, the frequency of the test signal will be tuned so that both M is sufficiently large and f_t is close to f_m .

To evaluate the proposed mismatch compensation technique, we apply a known single-tone test signal to the signal acquisition channels of the dual-rate ADC module. The sampling frequencies of the two ADCs are fixed at 1.2-Gsps (no dual-rate sampling is required for calibration), and the frequency of the test signal is set to have the $M = 997$ frequency relationship shown in (26). Figure 16 shows the waveforms reconstructed from the samples obtained from each ADC containing gain/phase mismatch. Compared to Figure 16(a), a significant gain mismatch is observed in Figure 16(b) because the bandwidth of the T/H amplifier used for the first signal acquisition channel is set to ≈ 5 -GHz on purpose. The frequency components of the test signal and the associated gain/phase mismatch measured in hardware experiments are listed in Table 2.

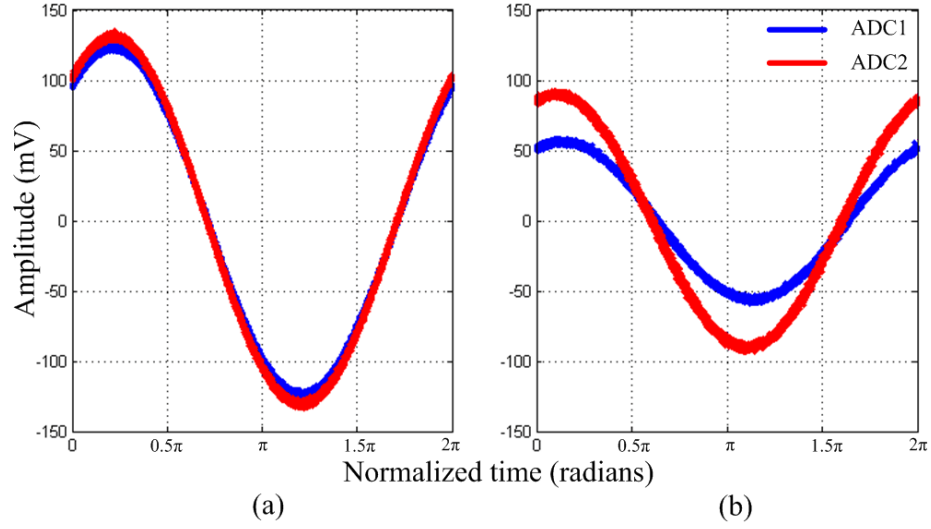


Figure 16: The signal reconstruction by fundamental frequency estimation for the test signal at (a) 275.6269MHz and (b) 6025.276MHz.

3.4.3 Evaluation

The frequency components of the multiband test signal defined in Table 3 are individually generated by RF signal generators (Agilent E4432B, E8257D) and combined with wideband power combiners. The generated test signal is fed to the signal acquisition module for dual-rate subsampling and the proposed signal reconstruction. We determine the optimal sampling frequencies as 1.2-GHz and 1.15-GHz, as described

Table 2: MISMATCH MEASUREMENT RESULT

| f_t (MHz) | f_m (MHz) | Gain Mismatch $ F_i $ | Phase Mismatch ϕ_i (rad) |
|-------------|-------------|-----------------------|-------------------------------|
| 275.6269 | 275 | 0.9421 | -0.0074 |
| 324.9749 | 325 | 0.9406 | -0.0105 |
| 1975.125 | 1975 | 0.9130 | 0.0563 |
| 2024.473 | 2025 | 0.9129 | 0.0548 |
| 2075.025 | 2075 | 0.9154 | 0.0622 |
| 2124.373 | 2125 | 0.9154 | 0.0666 |
| 6025.276 | 6025 | 0.6237 | -0.0918 |
| 6074.624 | 6075 | 0.6239 | -0.0909 |
| 6125.176 | 6125 | 0.6229 | -0.1078 |

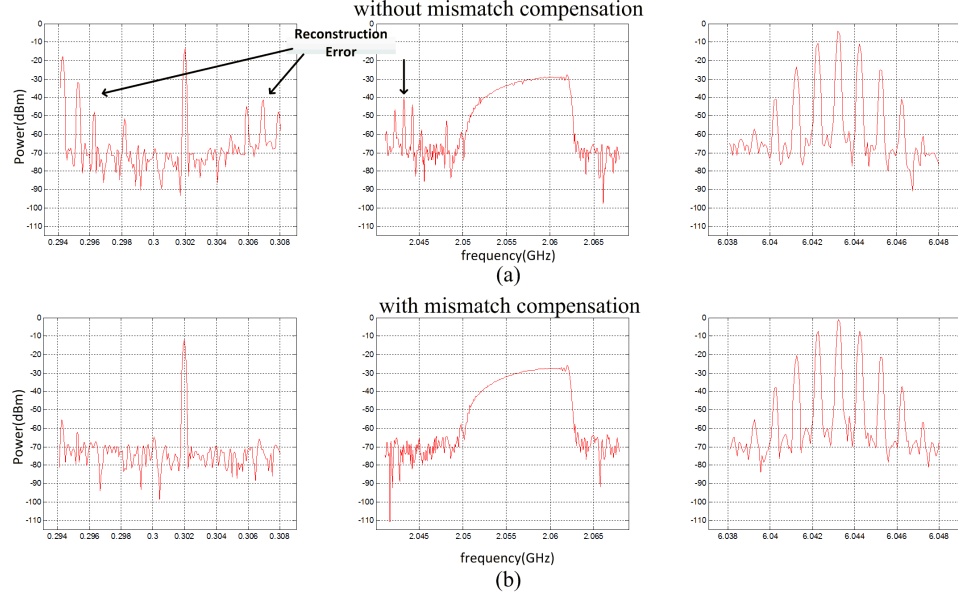


Figure 17: Signal reconstruction (a) without mismatch compensation and (b) with mismatch compensation.

Table 3: INPUT TEST SIGNALS FOR HARDWARE MEASUREMENT

| Band(GHz) | Type | f_c (GHz) | Dev.(MHz) | Rate(MHz) |
|--------------|-------------|-------------|-----------|-----------|
| [0.25, 0.33] | Single tone | 0.3 | NA | NA |
| [1.95, 2.15] | FM | 2.06 | 6 | 0.05 |
| [6.00, 6.15] | FM | 6.04 | 1 | 1 |

in Section 3.3, for the frequency contents of the test signal shown in Table 1. In this configuration, the bandwidth of the sub-band is $1/LT = 50\text{MHz}$. In Figure 17, the signal reconstruction without using the mismatch compensation technique (a) is compared to the waveform with compensation (b). The performance of the signal reconstruction without gain/phase mismatch compensation is significantly degraded because the channel mismatch is considerable in wideband signal acquisition, especially in the third band of the test signal. The test result shows that the mismatch compensation is necessary for the quality of signal reconstruction.

In Figure 18, each spectrum of the multiband test signal is individually measured with a spectrum analyzer (HP E4407B) for comparison with the signal reconstructed by the proposed signal acquisition technique. The three measured frequency bands

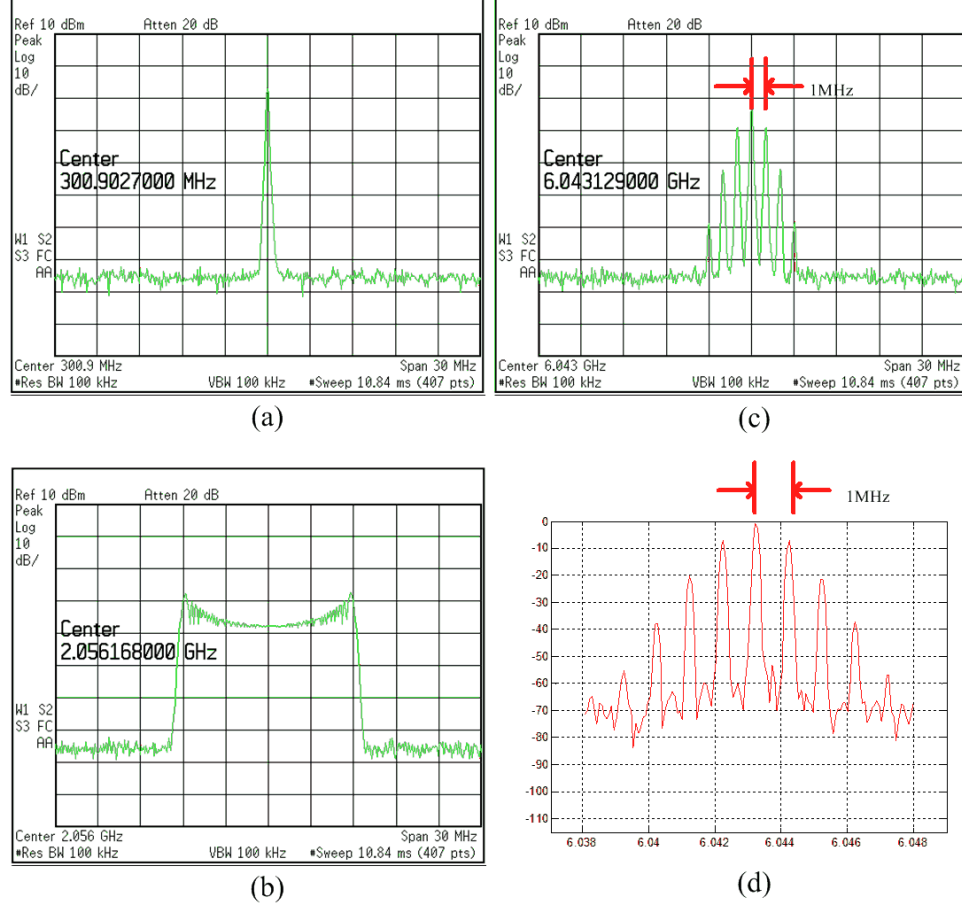


Figure 18: Comparison between the spectrum analyzer measurement (a), (b) and (c), and the proposed dual-rate undersampling measurement (d).

of the test signal are shown in Figure 18 (a), (b) and (c), where the frequency span is 30-MHz, and the frequency resolution is set to 100-kHz.

The third band of the test signal with frequency modulation (FM) is chosen for a closer look and for comparison between the spectrum measurement and the proposed signal acquisition. The spectrum analyzer measurement and the proposed dual-rate time-interleaved undersampling based measurement of the same FM test signal are shown in Figure 18(c) and Figure 18(d), respectively. As the FM rate of the test signal is 1-MHz, the spectra measured with the spectrum analyzer (shown in Figure 18(c)) contain a carrier component and an infinite set of side frequencies located symmetrically around the carrier frequency with the spacing of 1-MHz. The spectrum

obtained with the proposed sampling approach (shown in Figure 18(d)) resolves the frequency spacing as well as the measurement of the spectrum analyzer does.

3.5 Comparisons to Prior Works

To alleviate the practical concerns and cost of the conventional multicaset sampling, we propose a dual-rate sampling hardware system consisting of only two sampling modules to implement nonuniform periodic sampling. The use of a dual-rate sampler reduces additional sampling noise that may be introduced by hardware non-idealities or configuration mismatches among multiple samplers, which in turn compromises the signal integrity of signal acquisition systems.

In this section, the propose work is compared with the prior works on blind multi-band signal reconstruction.

Random demodulator and Modulated Wideband Converter (MWC) [61, 41]. In this approach, the signal is modulated by mixers in analog front-end (a single channel in [61] and a bank of modulators in [41]) to alias the spectrum into baseband. Then, the signal is reconstructed by solving the infinite measurement vectors (IMV) problem. However, the quality of the reconstruction is limited by the front-end RF components. The real mixer can create unwanted harmonics in the output and power leakage from local oscillator (LO) side. Moreover, the calibration is another difficult issue in MWC scheme due to many-channel (20-100 channels). In our work, the signal is directly sampled by ADC without analog pre-processing. Only two channel is required to perform the reconstruction and therefore the calibration process is much easier and less time-consuming.

Delayed-based Multicaset [39]. This work mainly focuses on spectral support sensing problem, and assuming the multicaset sample is acquired by ideal delay module for each channel. In their simulated example, 16 channels are required to reconstruct 6.3GHz bandwidth signal. A practical delay module, however, has a limited dynamic range and step size. In our work, the dual-rate sampler is proposed to avoid the use of the delay modules.

Synchronous and asynchronous Multirate sampling [20, 64]. In these works,

multirate sampling architectures are proposed. The multirate scheme can be classified into two groups by phase synchronization. The propose work falls into synchronous multirate sampling. In [20], synchronous multirate sampling is used to detect the active signal bands location. The full signal reconstruction, however, is not proposed in this work. Moreover, the phase synchronization between the channels is assumed to be given. In [64], the phase synchronization is relaxed to be asynchronous, and both active bands sensing and signal characterization are presented. However, the signal characterization relies on the statistical estimation (cross-correlation between the multirate samples and total variation), which may cause incorrect results due to spectral aliasing and noise. The proposed work fully reconstructs the signal in the presence of spectral aliasing and noise. We also propose all-digital phase-synchronization scheme for multirate sampler.

3.6 Conclusion

For measurement and reconstruction of a wideband sparse signal, we have proposed a new undersampling signal acquisition technique composed of dual-rate sampling hardware and a multicoset signal processing algorithm. Because of a frequency offset of the dual-rate sampling, non-equispaced samples for multicoset algorithms are acquired without many sampling channels. We have derived an explicit equation that converts dual-rate sample sets into multicoset sample sets. As the configuration of the multicoset algorithm varies with the dual-rate sampling frequency, the optimal combination of the dual sampling rates is studied. The optimality of the sampling frequency configuration is verified by computer simulation. For hardware validation, the dual-rate sampling hardware is implemented. We present and solve the issues (phase synchronization and mismatch calibration) on the dual-rate sampling hardware. Hardware results are provided to demonstrate the performance of the proposed method compared to a commercial spectrum analyzer.

CHAPTER IV

HIGH-SPEED DIGITAL BIT SEQUENCES ACQUISITION AND JITTER TRACKING USING INCOHERENT SUBSAMPLING

4.1 Proposed Jitter characterization Technique

In this work, we propose a new algorithm for jitter characterization of PRBSs signals and eye-diagram reconstruction by jitter compensation based on incoherent subsampling. While incoherent subsampling suffers from spectral leakage due to the mismatch between the input test signal and the discrete Fourier transform (DFT) basis, the proposed algorithm efficiently resolves the spectral leakage problem using a back-end signal process. The software-enhanced incoherent subsampling method alleviates the need for synchronizing the sampling clock with the test input signal. The only requirement of this method is a sufficiently wide input analog bandwidth to incorporate the potentially wide spectrum of the input signal. In the proposed method, a PRBS input signal is incoherently subsampled without any information of the PRBS signal. The fundamental frequency dependent with the bitrate and the pattern length of the PRBS is detected in the first stage of the algorithm. The fundamental tone of the input is detected by multirate subsampling. Once the fundamental tone is picked, a single period of the PRBS is digitally reconstructed from the obtained raw samples using the algorithmic CR whose flowchart is shown in Figure 19. The algorithmic CR is composed of four steps: discrete fundamental frequency (f_d) coarse estimation, f_d fine estimation, f_d fine tuning by sparsity promotion, and discrete-time remapping. f_d coarse estimation uses a windowed DFT with digital pre/postconditioning techniques to coarsely estimate the discrete fundamental frequency of the sampled

input signal by locating a spectral peak in the DFT spectrum. f_d fine estimation uses selective DFT frames to obtain an enhanced f_d estimation. Then, the discrete-time remapping with the estimated f_d rearranges the indices of the raw samples in the discrete-time-domain, representing a single period of the input signal. Optionally, a more enhanced f_d estimation can be obtained by the f_d fine tuning that exploits spectral sparsity constrained optimization.

The jitter characteristics of the input PRBS is quantified by analyzing the discrete-time samples of the reconstructed signal comparing with a digitally generated self-reference signal. The self-reference signal is extracted from the reconstruction itself by applying wavelet-based denoising. As this reference signal removes the need for externally provided analog reference signals, the complexity and the cost for the hardware synchronization will be reduced.

4.1.1 Incoherent Subsampling

Coherent sampling is satisfied when the entire samples contains an integer number of cycles of the input signal. It guarantees that the input signal power in the DFT domain is contained in one DFT bin. When an input signal whose frequency is unknown and time-varying due to its jitter (including frequency drifting by the absence of the synchronization with the sampling clock) is subsampled, it is called 'incoherently subsampled'. Thus, incoherent subsampling does not assume a common time-base between the input signal and the sampling clock. However, the analog input bandwidth of the digitizer should be wide enough to accommodate most of the significant frequency components of the input signal.

Suppose a continuous-time input PRBS signal is given by

$$x(t) = x(t - T_x(t)) + n(t), \quad (27)$$

where $T_x(t)$ denotes the unknown and time-varying jitter of the PRBS input signal, and $n(t)$ denotes additive white Gaussian noise. When the pattern length of the

PRBS is l and its bitperiod is T_b , the pattern repeats every $l \cdot T_b$ resulting in a periodic signal. The autocorrelation function of the signal is a triangle-pulse train whose period is $l \cdot T_b$. As a result, the power spectral density (PSD) of the PRBS, or the Fourier transform of the autocorrelation function of the PRBS, contains a delta-pulse train enveloped by sinc^2 . The space between the pulses corresponds to the fundamental frequency $1/(l \cdot T_b)$. In comparison with the continuous PSD, the discrete PSD of an incoherently subsampled PRBS suffers from signal aliasing and spectral leakage. Locating the frequency of the fundamental tone (f_d), however, is challenging due to the complex and rich spectrum of the discrete PSD. The remainder of this section introduces a new method for precisely estimating f_d .

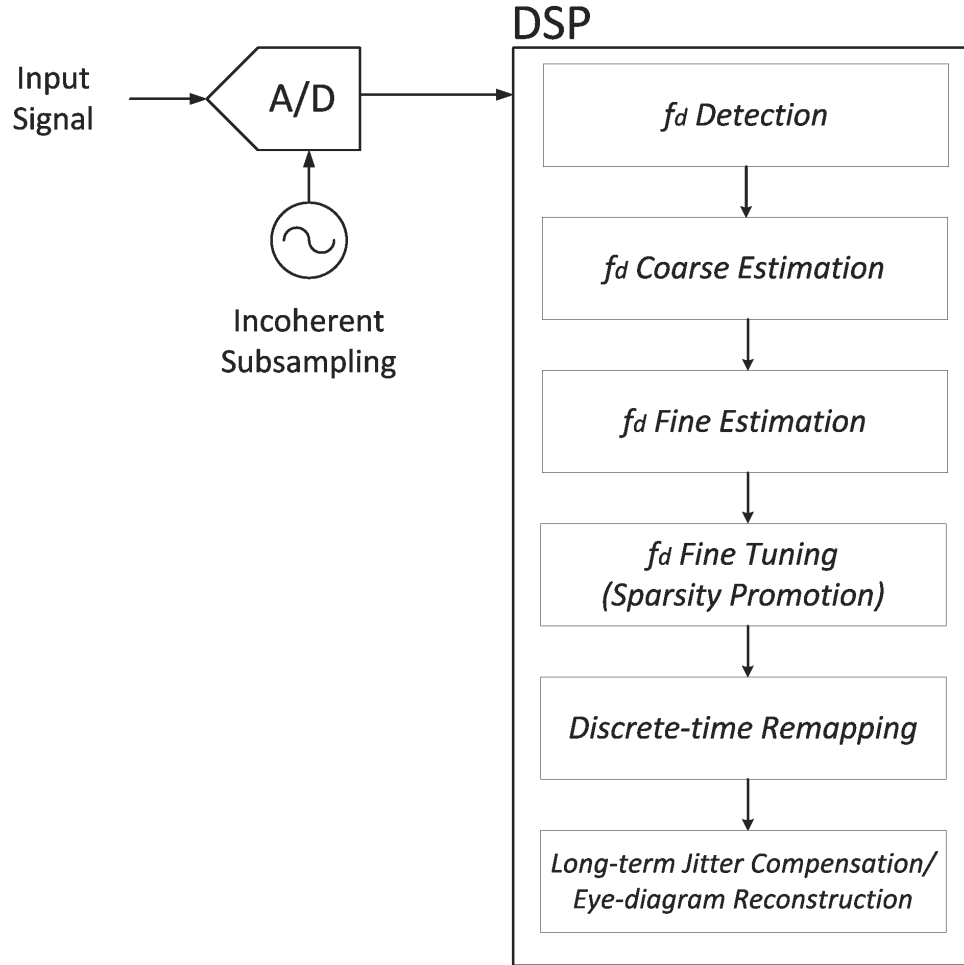


Figure 19: Block diagram of the proposed jitter characterization method.

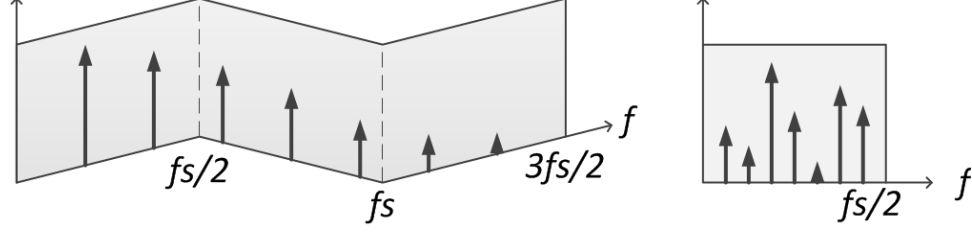


Figure 20: Subsampling the original spectrum effectively folds the frequency domain by $f_s/2$ and results in aliasing tones.

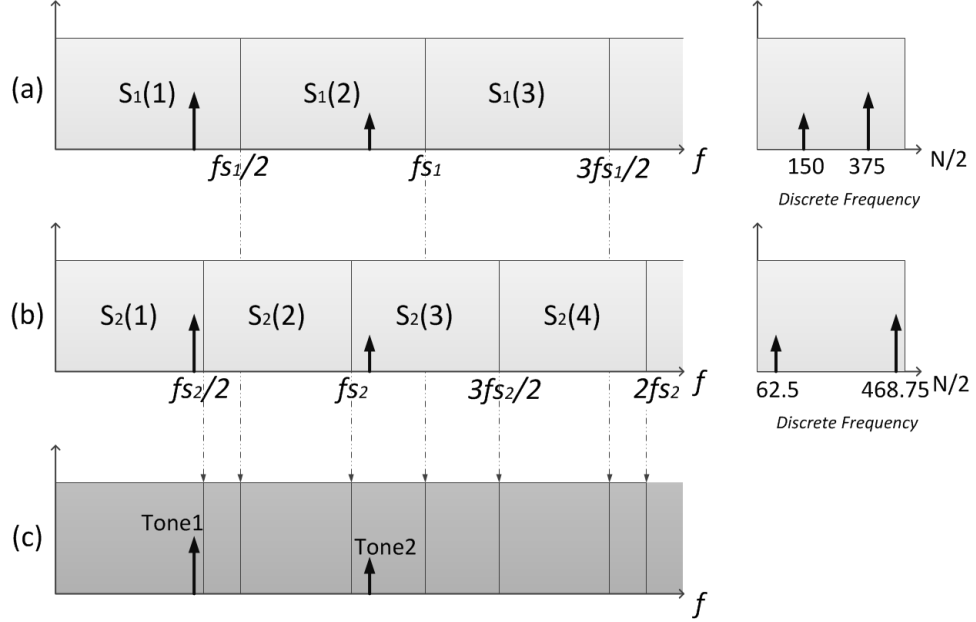


Figure 21: Examples of multirate sampling rates. Different discrete spectra are achieved in the discrete frequency domain from the same original test signal.

4.1.2 Detection of f_d : Multirate Subsampling

Multirate subsampling is used to detect f_d . The original continuous PSD of the signal is “scrambled” in the discrete frequency domain due to the frequency aliasing effect as shown in Figure 20. Subsampling can be thought as folding the continuous frequency domain by the half of sampling rate, $f_s/2$, referred to as the Nyquist zone [43]. Note that the resulting aliased spectrum is dependent on the sampling rate f_s .

Let f_{s1} and f_{s2} be two different sampling rates where $f_{s1} > f_{s2}$. Then, for the same analog test signal, two different sampling rates generate two different DFT

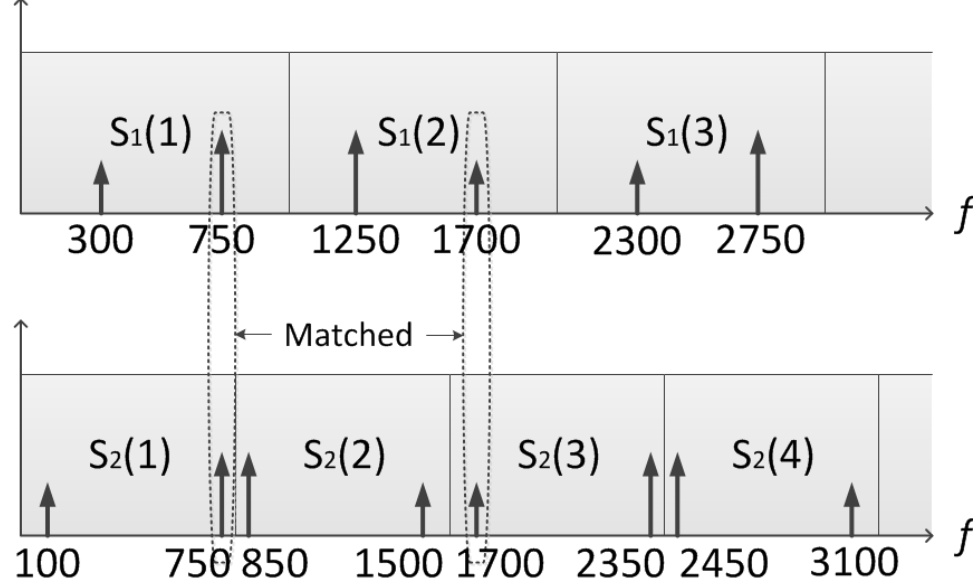


Figure 22: Spreading DFT spectra by multirate and converting to analog frequency. In this example, two tones at 750MHz and 1700MHz are matched.

spectra as shown in Figure 21. Unless the continuous PSD components are overlapped in the discrete frequency domain, “unfolding” the aliased discrete spectrum will provide the information about the original PSD components. Figure 22 shows the “unfolding” process of the aliased DFT spectra sampled at two different sampling rates. Before describing the proposed unscrambling method in detail, let us first consider a simple and intuitive example.

Example: We will first illustrate how the analog frequency of the signal converts into the discrete frequency. Suppose a signal contain two tones at $f_{t1} = 750\text{MHz}$ (T1) and $f_{t2} = 1.7\text{GHz}$ (T2) as shown in Figure 21(c). The signal is sampled at two different sampling rates, $f_{s1} = 2\text{GHz}$ and $f_{s2} = 1.6\text{GHz}$, and the number samples for DFT is $N = 1000$ for both cases. For the first sampling rate ($f_{s1} = 2\text{GHz}$), T1 and T2 are located in the first and the second Nyquist zone, respectively. Note that T2

is aliased. The discrete frequency ¹ of the two tones are

$$D_{t1,s1} = |750 - 0| \cdot \frac{1000}{2000} = 375, \quad (28)$$

$$D_{t2,s1} = |1700 - 2000| \cdot \frac{1000}{2000} = 150. \quad (29)$$

Similarly, for the second sampling rate ($f_{s2} = 1.6\text{GHz}$), T1 and T2 are located in the first and the third Nyquist zone, respectively. The discrete frequency of the two tones are

$$D_{t1,s2} = |750 - 0| \cdot \frac{1000}{1600} = 468.75, \quad (30)$$

$$D_{t2,s2} = |1700 - 1600| \cdot \frac{1000}{1600} = 62.5. \quad (31)$$

Note that the discrete frequency above is normalized to N , not 2π .

The idea of recovering the original frequency is listing all the possible analog frequencies based on the two discrete spectra sampled at two different clock rates and then finding the common frequencies. The two DFT spectra are converted and unfolded in the analog frequency domain as shown in Figure 22. $S_1(n)$ and $S_2(n)$ denotes the n -th Nyquist zone of the first and the second sampling rate, respectively.

For example, the possible analog frequencies of $D_{t2,s1}$ is obtained by

$$\left. \begin{aligned} \frac{2000}{1000} \cdot 150 &= 300\text{MHz}, \\ \frac{2000}{1000} \cdot 150 + 2000 &= 2300\text{MHz} \dots \end{aligned} \right\} \text{ odd Nyquist zone} \quad (32)$$

$$\left. \begin{aligned} 2000 - \frac{2000}{1000} \cdot 150 &= 1700\text{MHz}, \\ 4000 - \frac{2000}{1000} \cdot 150 &= 3700\text{MHz} \dots \end{aligned} \right\} \text{ even Nyquist zone} \quad (33)$$

In similar way, we can list the possible analog frequencies of $D_{t2,s1}$, $D_{t1,s2}$ plotted in Figure 22. The tones around 750MHz and 1700MHz are matched, indicating the frequencies of the two tones in the test input signal. These tones are referred to as “matched frequencies”.

¹The discrete frequency is normalized to N in this section simplicity's sake, unless otherwise specified. After this section, we will return to the 2π -normalized discrete frequency.

We now generalize the example. Let $\hat{p}(i)$ and $\hat{q}(i)$ be the discrete frequency of the i -th tone in the DFT sampled at f_{s1} and f_{s2} , respectively. Note that $\hat{p}(i)$ and $\hat{q}(i)$ are positive integers in $[0, \frac{N}{2}]$ where N is the number of samples of the DFTs. Then, we can define unfolding the discrete frequencies, $\hat{p}(i)$ and $\hat{q}(i)$, to analog frequency domain as follows:

$$P_{odd}(i) = \{p | p = f_{s1}(k-1) + \frac{f_{s1}}{N}\hat{p}(i), \quad k = 1, 2, \dots\}, \quad (34)$$

$$P_{even}(i) = \{p | p = f_{s1}k - \frac{f_{s1}}{N}\hat{p}(i), \quad k = 1, 2, \dots\}, \quad (35)$$

$$P(i) = P_{odd}(i) \cup P_{even}(i), \quad (36)$$

$$Q_{odd}(i) = \{q | q = f_{s2}(k-1) + \frac{f_{s2}}{N}\hat{q}(i), \quad k = 1, 2, \dots\}, \quad (37)$$

$$Q_{even}(i) = \{q | q = f_{s2}k - \frac{f_{s2}}{N}\hat{q}(i), \quad k = 1, 2, \dots\}, \quad (38)$$

$$Q(i) = Q_{odd}(i) \cup Q_{even}(i), \quad (39)$$

where $P_{odd}(i)$ and $P_{even}(i)$ denote the set of the analog frequencies unfolded from the i -th discrete tone sampled at f_{s1} to the odd Nyquist zone and the even Nyquist zone, respectively. Likewise, $Q_{odd}(i)$ and $Q_{even}(i)$ denote the set of the analog frequencies unfolded from the i -th discrete tone sampled at f_{s2} to the odd Nyquist zone and the even Nyquist zone, respectively. The total unfolded spectra combining the odd and the even Nyquist components at f_{s1} and f_{s2} are denoted by $P(i)$ and $Q(i)$, respectively. Figure 22 illustrates the unfolded spectrum.

Note that the tones might not be exactly matched at the same frequency as in Figure 22 because the spectral leakage across the DFT frequency bins causes estimation errors in the conversion to analog frequency from digital frequency. Even though the resolution of the estimation is not very fine, the coarse frequency of the tones can be determined by comparing the unfolded DFT spectra from different sampling rates and searching the common frequencies in the spectra. However, it is not guaranteed that the matched frequencies will always be the correct frequencies of the input tones. In the given example, if we look further into higher frequencies, other

frequencies are matched at 6300MHz, 7250MHz, and so on. To reduce the unwanted matched-frequencies, another sample set at a different sampling rate is added, $f_{s3} = 1.8\text{GHz}$ for this example. Then, the lowest unwanted matched-frequency becomes 14.3GHz. In practical situation assuming the input test signal is bandlimited, we can apply an upper frequency bound which excludes unreasonable matched frequencies. This criterion is used to limit the search for matched frequencies originating from frequency “unfolding”.

When the input signal is a PRBS signal, its fundamental frequency is more likely to be located near the low end of the frequency spectrum. This is because the fundamental frequency of PRBS with the bit period of l and the bit rate of f_b is l/f_b and the rest of tones are simply harmonics of the fundamental tone [24]. In other words, a longer-bit-period-PRBS has a lower fundamental frequency. For this reason, it is sufficient to unfold the discrete DFT spectrum to just a few orders of the Nyquist zone. Thus, the integer k described in (34), (35), (37), and (38) can be a finite number. Once the frequency location of the PRBS spectrum near the baseband are determined, we can find the lowest frequency value among several matched-frequencies to locate the fundamental frequency. We denote the detected fundamental frequency \hat{f}_{detect} which can be described as

$$\hat{f}_{detect} = \min \left(\left(\bigcup_{i=1}^{n_1} P(i) \right) \cap \left(\bigcup_{i=1}^{n_2} Q(i) \right) \right), \quad (40)$$

where the number of tones detected in the DFT sampled at f_{s1} and f_{s2} is n_1 and n_2 , respectively.

4.1.3 Coarse Estimation of f_d : Windowed DFT and Spectral Interpolation

In this section, f_d is estimated by locating the fundamental spectral peak in the DFT spectrum. The spectral peak corresponding to f_d may consist of a few adjacent spectral components, not a single spectral bin, due to the spectral leakage by the

incoherency of sampling. The spectral leakage can be alleviated by applying a window function to the samples. In coarse estimation, the Gaussian window function is used because the combination with the Gaussian interpolation in the frequency-domain results in the lowest frequency estimation error [22]. The Gaussian window vector, $\mathbf{w} = [w[1] \ w[2] \ \dots w[n]]^T$, is defined as

$$w[k] = e^{-(k-n/2)^2/(2\sigma^2)}, \quad k = 1, 2, \dots, n, \quad (41)$$

where $\sigma = 1/8$. The length- n signal sample is time-windowed as

$$\mathbf{x}_w = [w[1]x[1] \ w[2]x[2] \ \dots w[n]x[n]]^T. \quad (42)$$

The Gaussian windowed-DFT magnitude spectrum of the length- n sample \mathbf{x} is given by

$$\mathbf{S}_0 = |\Phi^T \mathbf{x}_w|, \quad (43)$$

where Φ is the DFT matrix defined as

$$\Phi = [\mathbf{e}(0)\mathbf{e}(\Delta_f)\mathbf{e}(0)(2\Delta_f) \ \dots \ \mathbf{e}(0)(2\pi - \Delta_f)]. \quad (44)$$

A normalized DFT vector is given by

$$\mathbf{e}(\omega) = \frac{1}{\sqrt{n}} [1 \ e^{j\omega} \ e^{j2\omega} \ \dots e^{j\omega(n-1)}]^T, \quad (45)$$

where ω is angular frequency defined in $[0, 2\pi)$.

To estimate f_d , three-point interpolation [22] is used. The Gaussian interpolation formula is applied as

$$\hat{f}_{coarse} = \Delta_f \cdot \left(m + \frac{\ln(\frac{S_0[m+1]}{S_0[m-1]})}{2 \ln(\frac{S_0[m]^2}{S_0[m+1]S_0[m-1]})} \right), \quad (46)$$

where $S_0[m]$ is the spectral magnitude at the frequency index m .

The f_d estimation described above uses a simple spectral interpolation that increases the accuracy of frequency estimation. However, the estimation relies on the assumption that the envelope of the spectrum is Gaussian-shaped, which limits the accuracy of the estimation.

4.1.4 Fine Estimation of f_d : Selective DFT frame

In this section, we introduce a new method to further enhance the spectral resolution from the Gaussian interpolation. A DFT frame [18] is one of the popular approaches to reduce the digital spectral leakage and increase the accuracy of frequency estimation in compressive sensing. This method replaces the DFT basis with a redundant frame of sinusoids. Unlike the compressive sensing uses the DFT frame for sparse approximation and compressive sensing recovery, we apply the DFT frame to the limited frequency range around \hat{f}_{coarse} (the estimation in the previous stage). This selectively applied analysis helps reducing computational burden. The enhanced spectral resolution by the DFR frame is given by

$$\Delta_f(c) = \frac{2\pi}{cn}, \quad (47)$$

where c is defined as the oversampling factor. Then, the selective DFT frame is defined as

$$\Phi(c, p) = [\mathbf{e}(\omega' - p\Delta_f(c)), \dots, \mathbf{e}(\omega' - \Delta_f(c)), \mathbf{e}(\omega'), \mathbf{e}(\omega' + \Delta_f(c)), \dots, \mathbf{e}(\omega' + p\Delta_f(c))], \quad (48)$$

where $\omega' = 2\pi\hat{f}_{coarse}$ and p is a positive integer for the selected frequency range. The oversampling factor c allows to achieve c times finer frequency resolution than the conventional spectral resolution. The enhanced magnitude spectrum of the signal with the selective DFT frame is now given by

$$\mathbf{S}(c, p) = |\Phi(c, p)^T \mathbf{x}_w|. \quad (49)$$

In Figure 23, a computer simulation example is illustrated. A 3.23-Gb/s 127bit PRBS is subsampled at 1GHz sampling clock, and 2048 discrete samples are obtained. The figure shows a DFT-frame-based magnitude spectrum spanning a discrete frequency range of Δ_f centered at \hat{f}_{coarse} ($c = 64$ and $p = 32$). This example shows

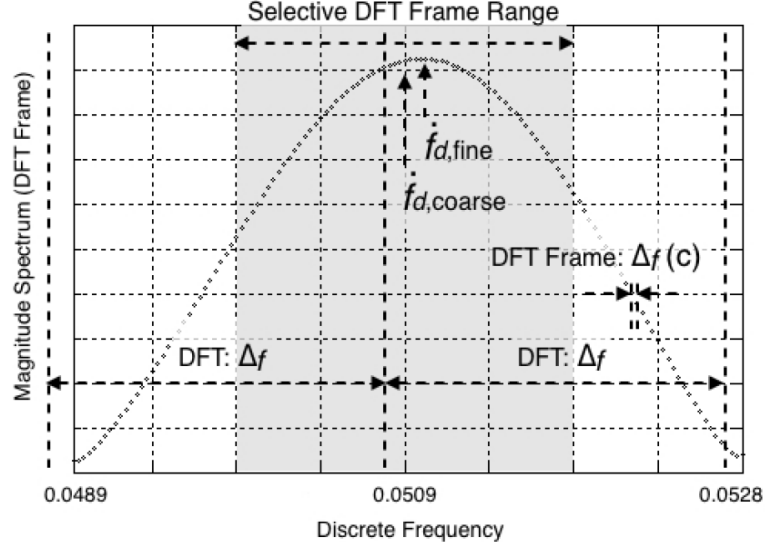


Figure 23: DFT-frame-based magnitude spectrum of a 3.23-Gb/s 127bit PRBS sub-sampled at 1GHz sampling clock.

that \hat{f}_{coarse} was not a local maximum of the magnitude spectrum. A new f_d estimation (\hat{f}_{fine}) is now obtained by searching the local maximum value of the enhanced magnitude spectrum as

$$\hat{f}_{fine} = \arg \max_r \left(\hat{f}_{coarse} + \Delta_f(c) \cdot r \right). \quad (50)$$

In addition, the use of iterative methods is plausible because the envelope of the DFT-frame-based magnitude spectrum is smooth and can be modeled as a continuously differentiable function.

4.1.5 Discrete Time Re-mapping

The sampled signal $x[n]$ is remapped to form the signal over a single fundamental period of the signal. As the estimated frequency (or period) is in the discrete domain, the period is normalized to 2π . By the discrete-frequency-to-time-conversion introduced in [13], discrete time of a sampled signal is determined as

$$t_d[k] = \text{mod} (t_d[k-1] + \hat{f}_{ind}, 2\pi), \quad k = 2, 3, \dots, n, \quad (51)$$

where $t_d[1] = 0$.

The re-mapped signal can be viewed as an oversampled signal with a single period of time. Note that the sampling space is not equally spaced. The spectral interpolation is still limited by the given spectral resolution Δ_f and the potential presence of the aliased tones adjacent to the fundamental tone. In the next step, the estimation resolution is further enhanced.

4.1.6 Fine Tuning of f_d : Sparsity Promotion Using a Spectral Jitter Cost Function

In this section, we introduce a technique that helps further reduce the amount of reconstruction errors observed in the previous fine estimation. The selective DFT frame-based estimation still limited by the given spectral resolution and the potential presence of the aliased tones adjacent to the fundamental tone due to the subsampling. In Figure 24(a), a 3.23-Gb/s 127-bit PRBS is subsampled at 1GHz clock and re-mapped to the discrete-time-domain by f_d fine estimation. The re-mapped waveform still contains timing dispersion even without any jitter in the simulation.

In fine tuning, the best estimation of f_d is found by searching for the f_d where the spectral leakage of the discrete spectrum of the reconstructed PRBS is minimized. This approach is enabled by the fact that a reconstructed signal that contains time dispersion due to errors in estimating \hat{f}_{fine} results in additional spectral leakage in the discrete spectrum. In other words, a reconstructed signal with the sparsest spectrum is considered the optimal reconstruction.

However, the spectrum evaluation of the reconstructed signal requires modification of the existing spectral analysis designed for equally spaced samples (the standard DFT) since the reconstructed signal contains non-equispaced samples. As one of the available non-equispaced DFT algorithms [29] based on interpolation is not computationally efficient, we propose a selective non-equispaced spectral analysis. We construct the discrete spectral components at only a few pre-defined locations

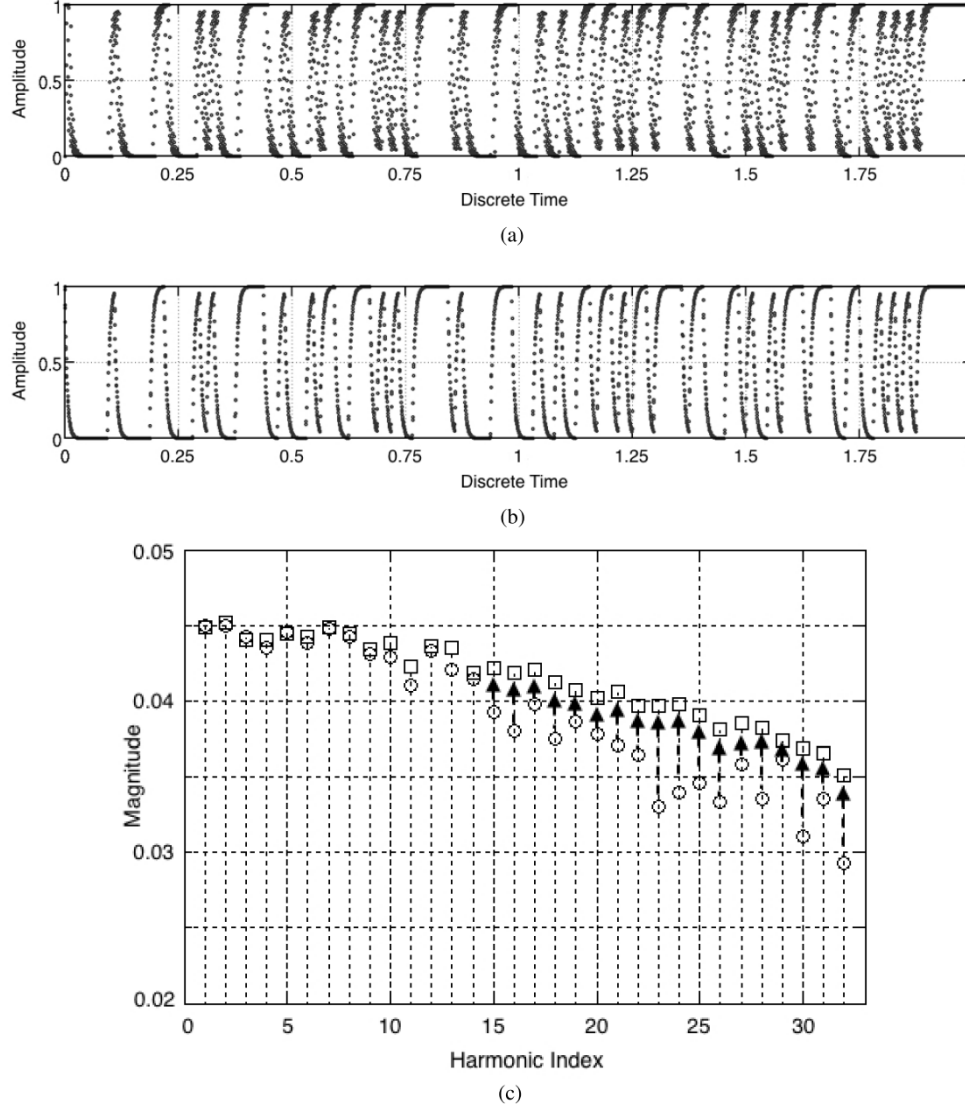


Figure 24: DFT-frame-based magnitude spectrum of a 3.23-Gb/s 127bit PRBS sub-sampled at 1GHz sampling clock.

of frequency bins, including the fundamental discrete frequency of the reconstructed signal and some of its m -th significant harmonics. The discrete Fourier basis functions required for evaluating discrete spectral components at the selective frequency

bins need to be re-defined for non-equispaced sample points as shown below

$$\mathbf{e}_1 \equiv \frac{1}{\sqrt{N}} [e^{-j2\pi t_d[0]/N} \quad e^{-j2\pi t_d[1]/N} \quad e^{-j2\pi t_d[2]/N} \quad \dots \quad e^{-j2\pi t_d[N-1]/N}]^T, \quad (52)$$

$$\mathbf{e}_2 \equiv \frac{1}{\sqrt{N}} [e^{-j2\pi 2t_d[0]/N} \quad e^{-j2\pi 2t_d[1]/N} \quad e^{-j2\pi 2t_d[2]/N} \quad \dots \quad e^{-j2\pi 2t_d[N-1]/N}]^T, \quad (53)$$

$$\dots \quad (54)$$

$$\mathbf{e}_m \equiv \frac{1}{\sqrt{N}} [e^{-j2\pi m t_d[0]/N} \quad e^{-j2\pi m t_d[1]/N} \quad e^{-j2\pi m t_d[2]/N} \quad \dots \quad e^{-j2\pi m t_d[N-1]/N}]^T. \quad (55)$$

The selective non-equispaced spectral analysis is performed as below:

$$\mathbf{\Psi} \equiv [\mathbf{e}_1 \mathbf{e}_2 \dots \mathbf{e}_m], \quad (56)$$

$$\mathbf{S} = \left| \mathbf{\Psi}^T \mathbf{x} \right|. \quad (57)$$

where \mathbf{x} is the length- N discrete samples of the input signal. Re-mapping process is not required because the frequency basis functions are already re-defined to accommodate the remapped discrete-time values. A time-windowing is not also used because the re-mapped sequence $t_d[k]$ represents a single period of the signal. Thus, the remapped samples are already coherent and does not produce any spectral leakage due to incoherency.

When the spectrum of the reconstructed signal is observed only in the selective frequency bins (the fundamental frequency and its harmonics), the sparsest total spectrum corresponds to the greatest sum of the spectrum magnitude at those selective frequency bins. This is because the optimal reconstruction corresponds to the reconstructed signal with the minimal discrete-time jitter or dispersion and it in turn results in the least spectral leakage in the frequency domain. In fine tuning, the sum of these spectrum magnitude is used as a cost function, called the spectral jitter cost function. The best reconstructed PRBS can be found by sweeping the discrete frequency in the range of $[\hat{f}_{fine} - \Delta_{f_{tune}}/2, \hat{f}_{fine} + \Delta_{f_{tune}}/2]$, where $\Delta_{f_{tune}}$ denotes the range of the discrete frequency sweep. Note that $\Delta_{f_{tune}}$ can be relatively small because \hat{f}_{fine} is already accurate. Among many different versions of the re-mapped

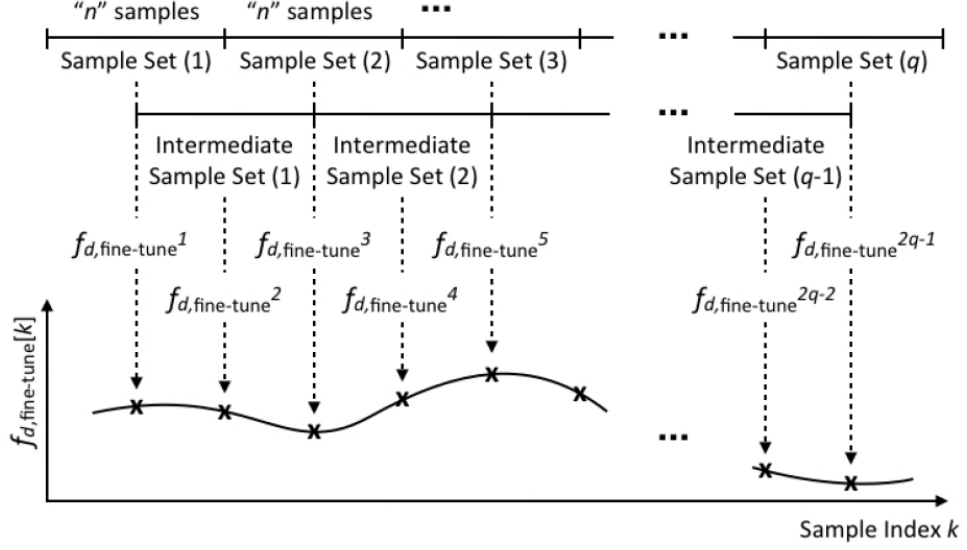


Figure 25: DFT-frame-based magnitude spectrum of a 3.23-Gb/s 127bit PRBS sub-sampled at 1GHz sampling clock.

discrete time sequence obtained by the fine tuning estimation, the one with the greatest sum of the \mathbf{S} 's results in the optimally reconstructed PRBS. In Figure 24(b), the re-mapped waveform by the fine tuning is shown. Compared to the waveform by fine estimation (Figure 24(a)), it contains less timing-dispersion. In Figure 24(c), the selective non-equispaced harmonic spectrum (the fundamental discrete frequency and its harmonics) is shown. The spectrum of Figure 24(a) is denoted by the circular marks and that of Figure 24(b) is denoted by the square marks. The fine tuning method is intended to find the optimal reconstruction by reducing the jitter quantity of the reconstructed signal whether the jitter originates from the signal itself or from the reconstruction errors. Therefore, the algorithm is efficiently reduces any timing dispersion in the sampled signal.

4.1.7 Long-term Jitter Tracking

An equivalent-time digital oscilloscope generally uses a clock signal that is phase/frequency synchronized with the input test signal as a sampling time-base. This sampling time-base signal contains almost the same long-term jitter content as that of the test signal.

For this reason, when the test signal is sampled by the synchronized sampling time-base, the long-term jitter of the test signal can be automatically cancelled out and barely measured by the oscilloscope. By contrast, the proposed jitter characterization technique does not incorporate any synchronization hardware. In this section, we propose a digital post-processing technique to track the long-term jitter contained in both the test signal and the sampling time-base.

Jitter is a value that accumulates over time, so it behaves as a random walk. The jitter time series is not bounded and contains long-term as well as short-term jitter components. In cases where long-term jitter components are predominant in overall jitter, a reconstructed waveform may contain discrete-time dispersion. We address this issue by tracking the long-term jitter components and compensating the reconstructed waveform.

For long-term jitter tracking, we measure the time-varying discrete frequency of the test signal where each frequency is obtained by the algorithm in the previous section. We use a sliding window that can be found in the short-time Fourier transformation (STFT), where the Fourier transform of local selections of the sampled signal is performed by a sliding time window. The estimated f_d may vary over the time windows due to the long-term jitter of the test signal. In this section, we use a timing-window that slides by $n/2$ sample points every frequency estimation, as shown in Figure 25.

4.1.8 Hardware Experiments

For hardware validation, a wideband subsampling digitizer is designed using a DC-18GHz wideband track-and-hold amplifier (Hittite HMC661LC4B) followed by a 12-bit A/D converter (Texas Instruments ADC12D1800), both set to run at 1-GSPS (Figure 26). In this scheme, the wideband track-and-hold amplifier is used as a front-end of the subsampling A/D converter to increase the input analog bandwidth of the

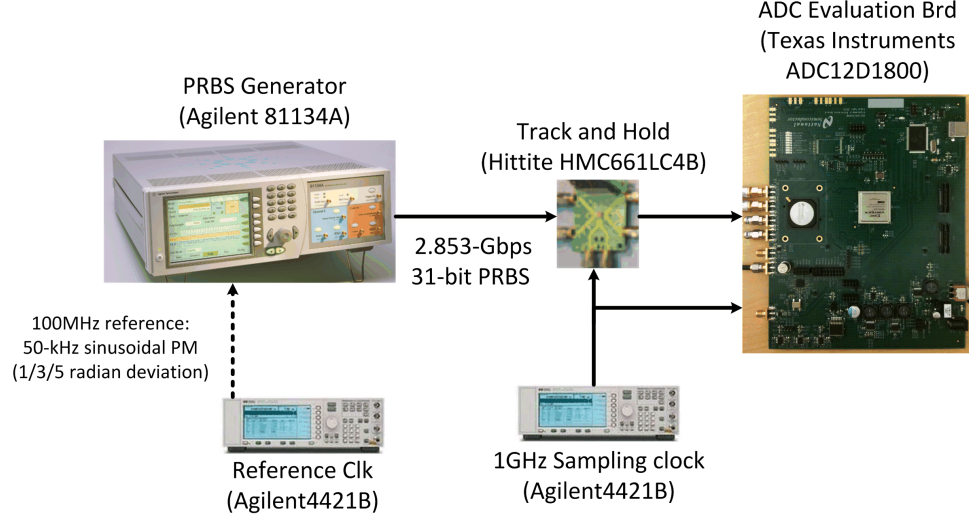


Figure 26: DFT-frame-based magnitude spectrum of a 3.23-Gb/s 127bit PRBS sub-sampled at 1GHz sampling clock.

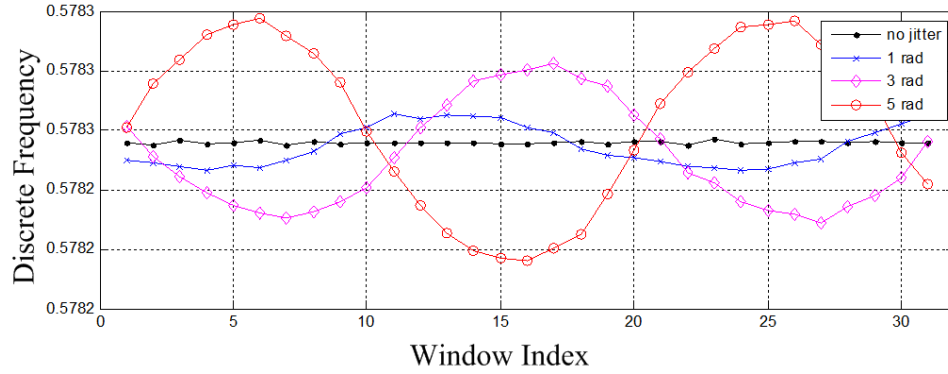


Figure 27: Short-time frequency estimation for PRBS test signals with sinusoidal jitter components.

digitizer system. The 2.853-Gbps 31-bit PRBS test signal is generated by a digital signal generator (Agilent 81134A) whose reference timebase is phase-modulated (sine) by using another signal generator (Agilent 4421B). The sampling clock signal of the digitizer is not synchronized in frequency with the test signal being sampled. This test setup is used for all the hardware validation processes in this section.

To evaluate the performance of the proposed frequency estimation method (or corresponding jitter tracking), we applied periodic jitter components (50-kHz sinusoidal phase modulation and 1/3/5 radian deviation) to the PRBS test signal and

measured the accuracy of frequency estimates digitally obtained from sampled signals. The total number of samples is $32 \cdot 1024$ and $2 \cdot 1024$ samples are used for a sliding window overlapped by 50%. Thus, 31 total sliding windows are used. The short-time frequency estimation for the PRBS with the sinusoidal jitter components is shown in Figure 27.

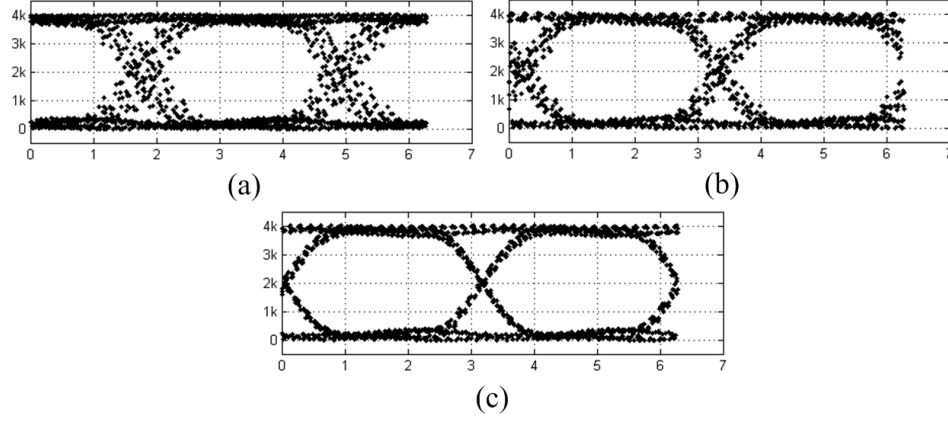


Figure 28: Comparison between eye-diagram. (a) The eye-diagram by a single sliding window (2048 samples) without tracking jitter components. (b) The eye-diagram by a single sliding window (2048 samples) by fine estimated jitter-tracking and (c) fine-tuning estimated jitter-tracking.

The performance of the jitter tracking is shown in Figure 28 for the 2048-sample window. In Figure 28(a), a reconstructed eye-diagram is shown without the jitter tracking compensation. In Figure 28(b) and (c), the jitter tracking compensation is performed by the fine estimation and by the fine-tuning estimation, respectively. The results show that the fine-tuning estimation compensates the most amount of jitters due to the accurate frequency estimation.

CHAPTER V

MONOBIT SIGNAL ACQUISITION AND TRANSIENT RESPONSE TUNING OF HIGH-SPEED SERIAL I/O SYSTEMS

5.1 Low-Cost Multi-Channel Testing of High-Speed Signals Using Monobit Receivers and Incoherent Subsampling

Multi-channel RF test system has received attention, as it is expected to lead a significant increase in testing time and throughput. One of application of the multi-channel RF test system is testing multiple-input multiple-output (MIMO) systems. However, achieving accurate testing with high-resolution ADCs introduces high-cost in the multi-channel test system. The effort on reducing the cost of ADCs motivates the development of single-bit or monobit receivers. The design and performance of monobit receivers for ultra-wideband communications are discussed in [25, 76]. The works, however, are restricted to over-sampling condition and symbol estimation for communication purpose. In [49, 55], high-precision eye-opening monitor (EOM) circuit and adaptive control scheme are developed. The combination of high-precision EOM and adaptive decision-point control scheme improves bit-error-rate (BER) [49]. In [55], a 10-Bs/s adaptive look-ahead decision feedback equalizer (LADFE) is used to measure eye-diagram and fabricated in 90-nm CMOS technology. Successive-approximation register (SAR) ADC is an attractive design for low-cost and low-power ADC. The SAR ADC determines the level of input signal through a binary search algorithm. However, SAR ADC with high-resolution need a large capacitor array which limits the ADC dynamic performance.

In this section, we consider a monobit receiver using clocked-comparator whose

threshold voltage is time-variant to increase the resolution of the ADC. By comparing the time-variant threshold voltage, the level of input signal is estimated. With a carefully chosen combination of sampling frequency and threshold frequency, the input signal is reconstructed with high-resolution. In [16], a similar idea which exploits a periodic threshold voltage (ramp signal) to compare with the input signal has been proposed. This work, however, requires the threshold signal and the input signal to be synchronized. In other words, the phase relationship of the two signals is known during the measurement. The main contribution of this work is in proposing a low-cost hardware scheme of monobit receivers to reconstruct a high-speed RF signal using intelligent incoherent subsampling and signal reconstruction algorithms. Since the algorithm is based on incoherent sampling technique, the phase of the input signal, the sampling clock signal and the threshold signal do not have to be synchronized. This property simplifies the hardware setup for the signal testing. In addition, the application of our algorithm is not constrained to digital bit sequences. It can also reconstruct any arbitrary periodic signal. Thus, the algorithm extends to testing RF harmonic signals. The overall architecture of the proposed method is presented in Section II. The detailed signal reconstruction algorithm is described in Section III. The optimal choice of the sampling frequency and the frequency of threshold signal is studied in Section IV. In Section V, hardware measurements with a FPGA board and a clocked-comparator show the results of the reconstruction.

5.1.1 Multi-Channel Monobit Receiver Architecture

The proposed multi-channel monobit-receiver architecture is shown in Figure 29. For each device under test (DUT), a single user I/O port receives a sequence of data logic from a clocked-comparator. The clocked-comparator converts the input test signal into two logic-levels (High or Low). A time-variant threshold signal is applied to the clocked-comparator and compared with the input test signal. If the input test signal

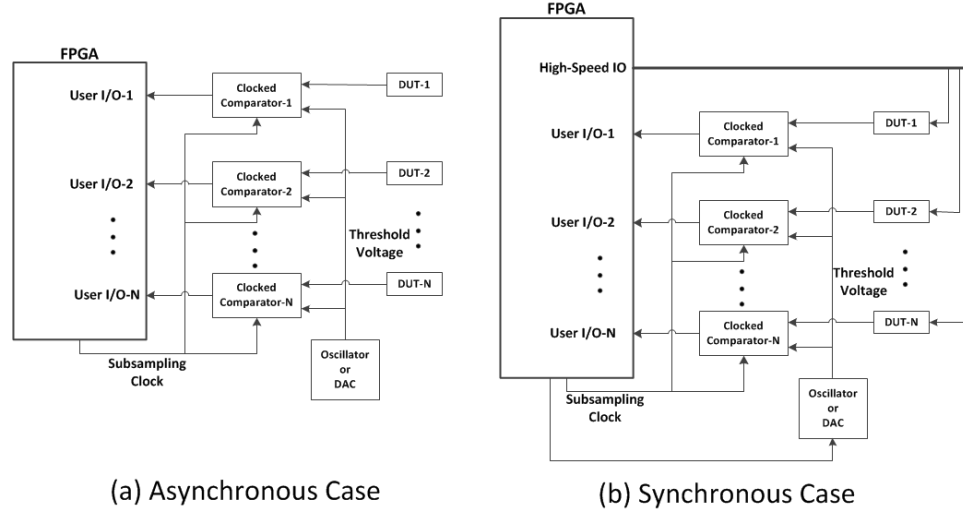


Figure 29: Block diagram of the multi-channel monobit-receiver test system: (a) The system is asynchronized with the DUTs and the DAC. (b) The system is synchronized with the DUTs and the DAC. The red signals highlight the synchronization.

is greater than the threshold signal, the output of the clocked-comparator is High. Otherwise, the output is Low. The threshold signal comes from an oscillator which generates a sin wave or from a DAC which provides any arbitrary waveform. The FPGA samples the bit stream with a subsampling clock which is also shared with the clock-comparator. A time-delay between the sampling clock of FPGA and the sampling clock of the clocked-comparator is adjusted to compensate the propagation delay of the clocked-comparator.

The threshold signal can be either synchronized or asynchronized with the system. The asynchronous case that the DUTs and the threshold signal are not synchronized with the main system is shown in Figure 29(a). In the asynchronous case, the back-end algorithm performs extra processes: estimation of the fundamental frequency of the input test signal (due to asynchronous DUTs) and digital phase adjustment of the threshold signal (due to asynchronous threshold signal). The threshold signal can be generated from an oscillator which produces a sin wave or from a DAC which can produce any arbitrary waveform. The constraint for the threshold signal is, however, that it should be periodic and its fundamental frequency should be carefully chosen

for the signal reconstruction. In addition, the peak-to-peak of the threshold signal embraces that of the input signal. This condition guarantees that the input test signal is fully covered by the threshold signal.

In Figure 29(b), the DUTs and the threshold signal are synchronized with the main system. In this setup, the synchronization issue is relaxed by the hardware itself. Therefore, the digital compensation is not required. In the synchronous case, the reconstruction algorithm is implementable in FPGA and outputs the result on-the-fly because the reconstruction logic is simpler than the asynchronous case. Thus, more applications such as TDR and online eye-monitoring are possible in the synchronous case.

5.1.2 Incoherent-Threshold Signal Reconstruction

Before illustrating the proposed algorithm, the notation of this paper is denoted as followings:

$$f_s = \frac{1}{T_s} : \text{ sampling clock frequency(Hz),} \quad (58)$$

$$f_{th} : \text{ threshold signal frequency(Hz),} \quad (59)$$

$$x(t) : \text{ input test signal,} \quad (60)$$

$$x[n] = x(nT_s) : \text{ n-th sample of input test signal,} \quad (61)$$

$$v(t) : \text{ threshold signal,} \quad (62)$$

$$v[n] = v(nT_s) : \text{ n-th sample of thershold signal,} \quad (63)$$

$$d[n] : \text{ n-th sample of clocked comparator output,} \quad (64)$$

$$\hat{f}_d : \text{ discrete fundamental frequency of input test signal.} \quad (65)$$

The input test signal ($x(t)$) and the threshold signal ($v(t)$) are sampled at the rising edge of the sampling clock with the frequency f_s . The two sampled points are

compared and the output logic level is determined as following:

$$d[n] = \begin{cases} 1, & \text{if } x[n] \geq v[n], \\ 0, & \text{if } x[n] < v[n]. \end{cases} \quad (66)$$

Note that 1 and 0 represent a voltage level, not the actual voltage value. The brief overview of the algorithm is as follows: 1) estimate the discrete fundamental frequency of the test input signal, 2) locate the samples over the discrete fundamental period with its discrete time, amplitude and logic level, and run iteratively while the digital phase of the threshold signal, $v[n]$, is adjusted with a cost function. 3) interpolate the boundary points of logic 1 and 0.

5.1.2.1 Step1- Estimate the fundamental discrete frequency

In [44], accurate discrete frequency estimation using the frequency shifting technique is presented. We use the frequency shifting technique to improve the resolution of the discrete fundamental frequency of the input test signal. The idea of the frequency shifting method is to shift (or modulate) the discrete spectrum of incoherent sampling to fit into the DFT frequency bins. When the discrete frequency of the fundamental tone is not exactly on a DFT bin, a spectral leakage happens into the neighbor bins. By shifting the fundamental tone close to the DFT bin, the magnitude of the corresponding DFT bin would increase. To compute the fundamental discrete frequency (\hat{f}_d) of the input signal, the ground reference is applied to obtain an one-bit resolution samples of the AC-coupled input test signal.

5.1.2.2 Step2- Locate samples

In this step, the amplitude-resolution of the input test signal is improved by comparing with the sinusoidal threshold signal. Since the amplitude and the frequency of the threshold signal are given, we can draw a virtual threshold signal without its exact phase. While the phase of the threshold signal is adjusted in the next process, we

assume the phase is known for the following example. Figure 30(a) shows an example of a square wave input test signal and a sinusoidal threshold signal. When the input test signal is greater than the threshold signal, the clocked-comparator generates the samples of logic 1. The grey downward-pointing triangles represent the samples of logic 1. Similarly, the black upward-pointing triangles represent the samples of logic 0. Note that the logic of the samples is flipped when the threshold signal crosses over the input test signal. The dotted-circles emphasize the boundary points of the flipping logic. The frequency of the threshold signal is carefully chosen to have a long common period with the input test signal. Otherwise the threshold signal travels only a few paths over the test signal, which reduces the resolution of the reconstruction. Once the \hat{f}_D is estimated in the previous step, the discrete time of $v[n]$ is determined over the fundamental period as shown in Figure 30(b). The time location of the k-th sample is remapped within the fundamental period as

$$t_d[k] = \text{mod}(k, N/\hat{f}_d), \quad (67)$$

where N is the total number of samples. The discrete amplitude of $x[n]$ is evaluated by the boundary points of logic 1 and 0. In the example, the nine dotted-circles which indicate the boundary points imply the shape of the input test signal. As the number of samples increases the time and amplitude resolution of the boundary points increases as shown in Figure 30(c).

5.1.2.3 Step3- Digital phase adjustment

The digital phase adjustment is achieved by iteratively changing the phase of the virtual threshold signal. Note that the phase of the true threshold signal is unknown. If the phase of the virtual threshold signal does not match the phase of the true threshold signal, the mismatch error occurs at the boundary points. Figure 31 shows the previous example with an incorrect digital phase offset. Comparing with Figure 30(b), the incorrect digital phase of the virtual threshold signal introduces the error from

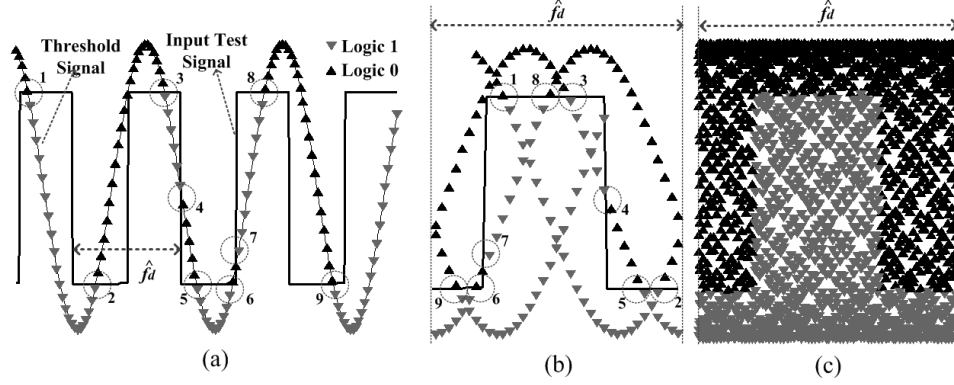


Figure 30: (a) A square wave and a sinusoidal threshold signal are plotted with the output logic of the clocked-comparator over the time axis. (b) The samples are remapped over the estimated \hat{f}_d . The circles indicate the flipping points. (c) More samples are plotted.

the boundary points to the input test signal as shown in Figure 30(a). As a result, the boundary points do not accurately cover the input test signal in Figure 30(b). Note that the envelopes of logic 1 and logic 0 exactly meet at the input test signal in Figure 30(c), while they cross over each other in Figure 30(b). The best phase of the virtual threshold signal is selected when the following cost function is minimized.

$$cost(\phi) = \int_0^{\hat{f}_d} env_0(u, \phi) - env_1(u, \phi) du, \quad (68)$$

where ϕ is the digital phase of the virtual threshold signal and u is a dummy variable in $[0, \hat{f}_d]$. The function $env_0(u, \phi)$ is the envelope of the logic 0 samples and $env_1(u, \phi)$ is the envelope of the logic 1 samples. The shape of the function $env_0(u, \phi)$ and $env_1(u, \phi)$ depends on ϕ .

5.1.2.4 Step4- Evaluate logic boundary

The final step of the algorithm is to evaluate the logic boundary. The logic boundary roughly indicates the input test signal. The envelope of the logic 0 (logic 1) samples is obtained by choosing the minimum (maximum) value in a given time window. Figure 32 shows an example to evaluate the logic boundary. Evaluating the logic

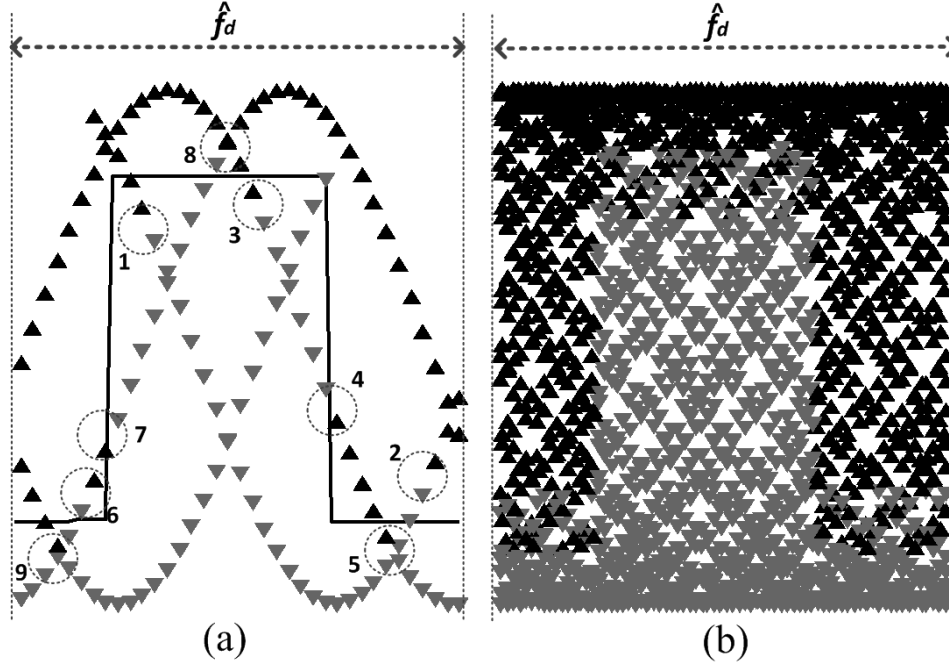


Figure 31: Incorrectly estimated digital phase of the threshold signal produces errors.

boundary with a short time window can improve the resolution over the time. However, the logic boundary can be over-evaluated with a too short time window. Thus, the size of time window should be carefully chosen based on the number samples.

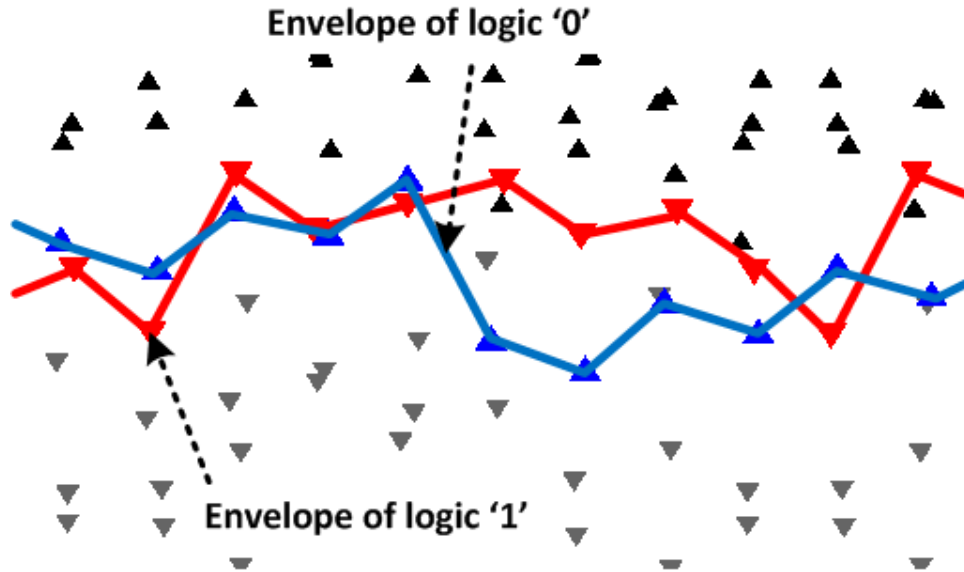


Figure 32: The logic boundary is evaluated by enveloping.

5.1.3 Frequency Selection

Given the input test signal, the frequencies of the sampling clock and the threshold signal determine the resolution of the reconstruction. As discussed in the previous section, the frequency relationship between the input test signal and the threshold signal decides the number of the distinct paths that the threshold travels over \hat{f}_d . As the number of the distinct paths increases, more number of amplitudes of the threshold signal is compared with the input test signal. Furthermore, the frequency relationship between the sampling clock and the input test signal impacts on the time resolution of the reconstruction.

All the relationship of the three frequencies (clock, input, and threshold) is desired to have a long common period. If they have a short common period, it takes a short time (or few samples) to sample the same point of the input test signal with the same point of the threshold signal. It means that the redundant information is obtained in a few samples. To avoid a short common period, we choose the frequencies of the sampling clock and the threshold signal with the fundamental frequency of the input test signal as following:

$$f_s = \frac{\prod_{i=1}^{P_1} \alpha_i}{\prod_{i=1}^{S_1} \beta_i} f_d, \quad (69)$$

$$f_{th} = \frac{\prod_{i=S_1+1}^S \beta_i}{\prod_{i=P_1+1}^P \alpha_i} f_d, \quad (70)$$

$$(71)$$

where $1 \leq P_1 \leq P$ and $a \leq S_1 \leq S$, and f_{th} are the frequencies of the sampling clock and the threshold signal, respectively. The fundamental frequency of the input test signal is denoted by f_d . Note that f_d is the continuous frequency whereas \hat{f}_d is the discrete frequency related to the total number of samples N . The integers $\alpha_1, \dots, \alpha_p$ and β_1, \dots, β_S represent the prime numbers. The set $A = \{\alpha_1, \dots, \alpha_p\}$

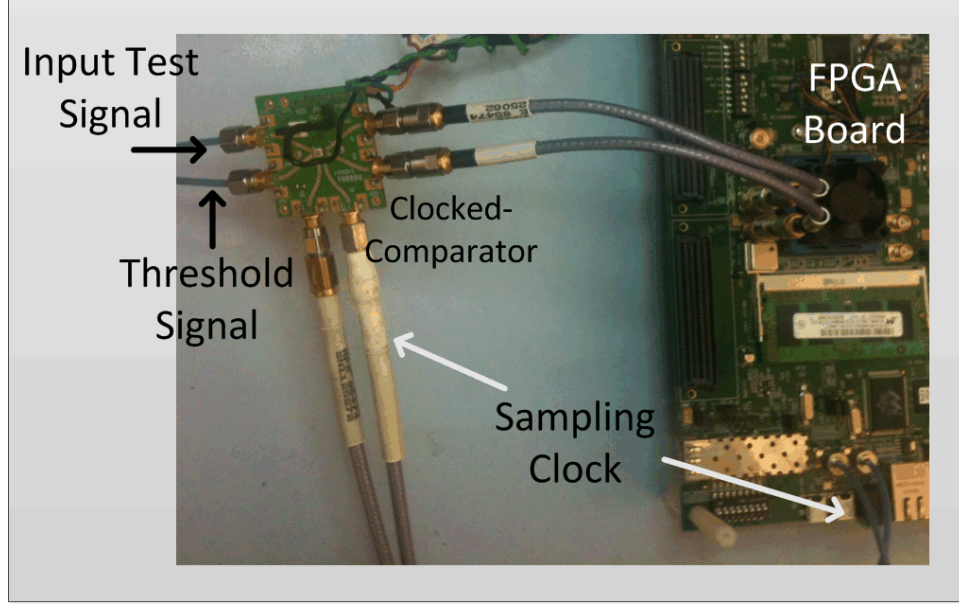


Figure 33: Hardware measurement setup.

and $B = \{\beta_1, \dots, \beta_S\}$ are chosen to be disjoint $A \cap B = \emptyset$, which leads

$$f_s = \frac{\prod_{i=1}^P \alpha_i}{\prod_{i=1}^S \beta_i} f_{th}, \quad (72)$$

without any cancellations. The time-resolution of the reconstruction is determined by $\prod_{i=1}^{P_1} \alpha_i$ and f_d . This is because the number of the time-stamps of the sample points in the fundamental period is $\prod_{i=1}^{P_1} \alpha_i$. Thus, the time-resolution is

$$res_t = \frac{1}{f_d \cdot \prod_{i=1}^{P_1} \alpha_i}. \quad (73)$$

5.1.4 Hardware Measurement

The measurement setup is shown in Figure 33. HMC874LC3C from Hittite is a clocked-comparator supporting 20Gbps clock operation and 10GHz input bandwidth. The output waveform of the clocked-comparator is captured by an FPGA board. We use a Virtex6 evaluation board. Two types of input test signals are measured: a digital square wave and a sin wave. The high-speed digital square wave of 1.6GHz frequency is generated. For the sampling clock,

$$f_s = \frac{163 \cdot 223}{977 \cdot 983} 1.6GHz \approx 60.557MHz, \quad (74)$$

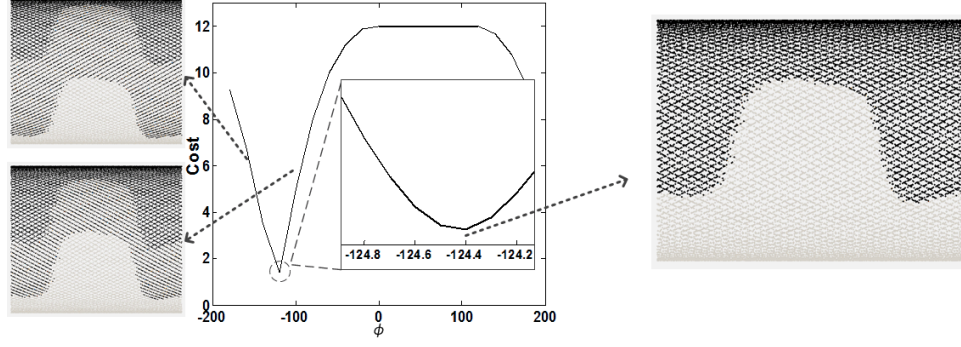


Figure 34: Cost function and remapped samples.

is chosen as the sampling frequency. The frequency of the sinusoidal threshold signal is chosen as

$$f_{th} = \frac{163 \cdot 223 \cdot 991^2}{977 \cdot 983 \cdot 997^2} 1.6GHz \approx 59.8303MHz. \quad (75)$$

Similarly, the frequencies of the sampling clock and the threshold signal are chosen for the 1GHz sin wave with different prime numbers as followings:

$$f_s = \frac{221 \cdot 223}{977 \cdot 983} 1GHz \approx 48.9937MHz, \quad (76)$$

$$f_{th} = \frac{221 \cdot 223 \cdot 991^2}{977 \cdot 983 \cdot 997^2} 1GHz \approx 48.4057MHz. \quad (77)$$

To cover the input test signal, the peak-to-peak of the threshold signal is set to 600mV. The threshold signal is applied externally without synchronization.

Figure 34 shows the cost function over the adjusted digital phase in the case of the square wave. While the phase is swept over the range $[-180, 180]$ degree, the cost function is computed. The cost function has the minimum value at the phase of -124.4 degree. The threshold signal of phase -124.4 degree produces least mismatches on the logic boundary.

Figure 35 compares the input test signal and the reconstructed signal. The envelopes of the logic 1 and logic 0 are plotted together. The result of the square wave input test signal shows the reconstructed signal has a minor distortion on the waveform. However, the reconstruction accurately captures the edge of the square wave

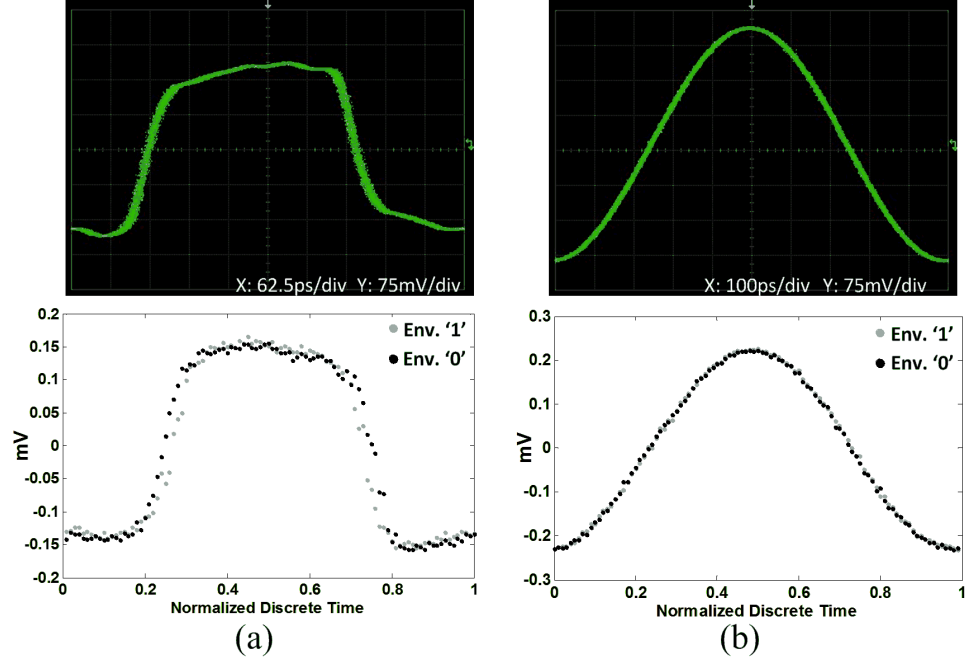


Figure 35: (a) Square wave and (b) sin wave input signal and reconstruction.

Table 4: TIME PARAMETER FOR HARDWARE MEASUREMENT

| | TR(ps) | TT(μ s) | NS |
|-------------|--------|--------------|-----|
| Square wave | 0.0172 | 338 | 20k |
| Sin wave | 0.0213 | 418 | 20k |

and the amount of jitter is very close to the signal measured by the high-speed oscilloscope. In sin wave measurement, the proposed algorithm reconstructs the waveform with better accuracy.

The results show the frequency of the sampling clock and the threshold signal does not require fast to reconstruct a high-speed input test signal. The input test signals measured in this paper are around 20 times faster than the sampling clock. The following table summarizes the time-resolution (TR), the test-time (TT) and the number of samples (NS) for the hardware measurements.

5.1.5 Conclusion and Future work

In this section, a new signal reconstruction architecture and algorithm is introduced. The hardware architecture with monobit receivers based on incoherent subsampling is

expected to reduce the cost of multi-channel testing. The use of a time-variant threshold signal increases the resolution of the signal reconstruction. The hardware measurement shows the input signal is reconstructed in high-resolution and high-accuracy without a synchronized threshold signal, which reduces the hardware complexity. In addition, the results show the reconstruction is achievable with low-speed sampling clock and threshold signal. In our future work, more robust method to reconstruct the input signal from the logic boundaries will be studied. The research to reduce the test-time will also be done. In addition, more algorithms for eye-diagram extraction will be included. Multi-channel testing system will be implemented in hardware with the proposed algorithm.

5.2 Multi-channel Testing Architecture for High-speed Eye-diagram Using Pin Electronics and Subsampling Monobit Reconstruction Algorithms

Multi-channel multi-Gbps digital I/O test systems are required to be equipped with channel monitoring capability to detect any failure or signal quality degradation while testing is being conducted. The potential channel failure includes connector wear-out, probe misalignment and the performance degradation of the device I/O. However, multi-channel pin electronics devices that are compatible with high-speed signaling and also equipped with channel monitoring functions are not readily available for tester development [46]. Cutting-edge field programmable gate arrays (FPGAs), which are widely used for the development of digital testers, are equipped with channel (or eye-opening) monitoring capability on their high-speed transceiver ports. However, the transceiver interface is not designed to be used as pin electronics. It is usually limited by its input dynamic range or dedicated to a particular type of signaling (i.e. differential signaling).

There are efforts to develop multi-Gbps PE (and eye-opening monitoring) chips. In [31], 8Gbps CMOS-PE macro was developed, which can be used for developing multi-channel test systems with eye-opening monitoring capability. In [25, 76], high-precision eye-opening monitor (EOM) circuit and adaptive control scheme were developed. The combination of high-precision EOM and adaptive decision-point control scheme improves the receiver sensitivity [76]. In [25], a 10-Gbps adaptive look-ahead decision feedback equalizer (LADFE) is used to measure eye-diagram and fabricated in 90-nm CMOS technology. However, in commercial area, pin electronics chips that can be purchased are mostly low-speed so not compatible with the frequency required for the cutting-edge digital device testing [49]. Tester design companies provide their own multi-channel high-speed pin electronics components and associated test systems, but such components may not be available for engineers and researchers outside their

research collaboration. For this reason, the development of low-cost multi-Gbps digital I/O test and measurement systems with advanced features such as eye-opening monitoring and channel characterization is needed.

We propose an FPGA-based multi-channel digital I/O test system with PE modules equipped with eye-opening monitoring capability using off-the-shelf components to reduce the overall development and test cost. 16 PE modules can be mounted on the test system, and the I/O of each module is connected to the high-speed transceiver of a back-end FPGA controller to enable multi-Gbps signaling. The PE module contains off-the-shelf components such as drivers, comparators, level-setting DACs and power splitters. In addition, a pattern/timing generator can be implemented with additional hardware and logics in the FPGA, but it is not part of this research. The overall architecture of the proposed method is presented in Section II. The detailed signal reconstruction algorithm is described in Section III. The optimal choice of the sampling frequency and the frequency of threshold signal is studied in Section IV. In Section V, hardware measurements with a FPGA board and a clock-comparator show the results of the reconstruction.

5.2.1 Approach

Figure 36 shows the proposed multi-channel testing architecture. The FPGA not only performs a transceiver but also provides a sampling clock for the clocked comparators and controls the DAC. The FPGA creates a multi-Gbps bit pattern through its high-speed IOs that dedicates to transmit a high-speed digital signal with the programmable logic resources. The high-speed bit pattern is re-transmitted by the driver that is a high-speed, low-jitter buffer with a programmable output swing and a programmable pre-emphasis. The DUT is stimulated by the high-speed bit pattern and the response signal is captured by the monobit receiver. The input response signal is subsampled and compared with the voltage level of the DAC that is controlled

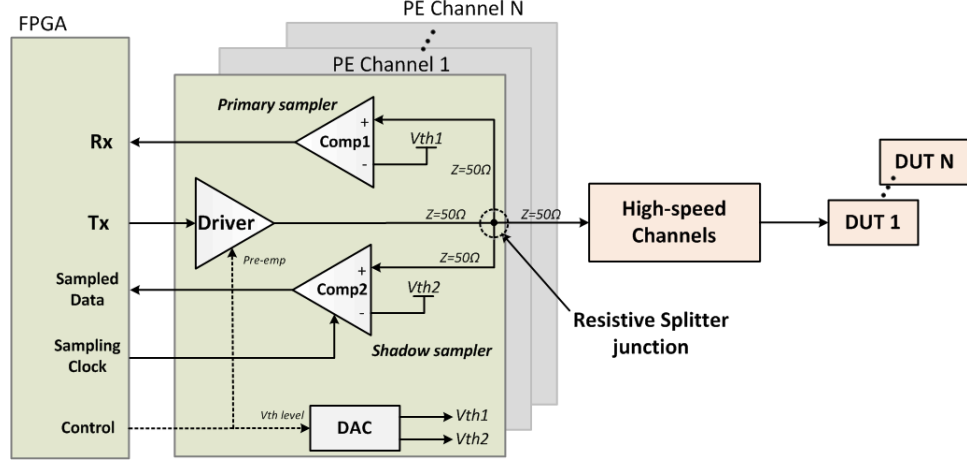


Figure 36: Block diagram of the proposed multi-channel testing system.

by the FPGA logic and synchronized with the subsampled clock signal.

One of the key contribution of this work is the high-speed input signal is reconstructed by the monobit receiver with very fine time and amplitude resolution using subsampling clock and a low-cost DAC. This feature enables the test architecture to have high-scalability because the hardware resource for a channel is minimized. The detail electronic features of the proposed architecture will be discussed in the next section.

5.2.2 FPGA test system hardware and Pin Electronics

A block diagram for the prototype test system is shown in Figure 37(a) and a photograph is shown in Figure 37(b). The test system is constructed on a printed circuit board that fits within the test head of a commercial ATE, taking up two of its standard expansion slots. On the bottom of the card are several multi-pin connectors that support communication buses and obtain power through the host ATE back-plane. Central to the design is a Xilinx "Kintex-7" 28nm CMOS FPGA that serves as a local test controller for the card. The FPGA receives test pattern data, test control parameters, and high-level commands from the host ATE. Otherwise, the FPGA performs the desired tests autonomously, without real-time interaction with

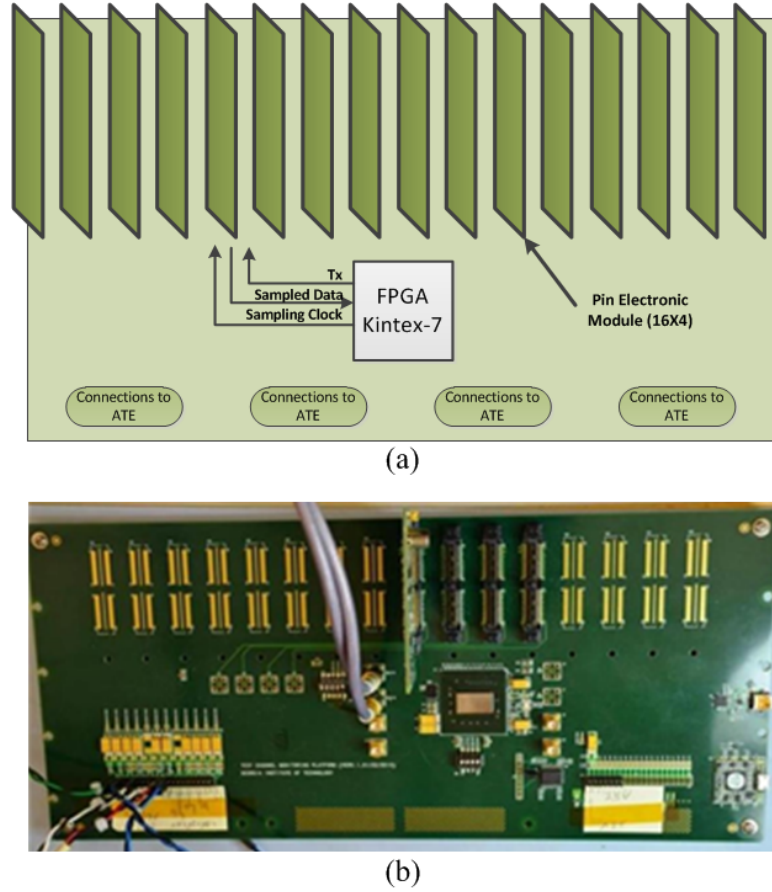


Figure 37: FPGA-based test system on a printed circuit board, (a) block diagram and (b) photograph of the prototype PCB.

the host ATE. Essentially the FPGA is programmed to act as a stand-alone local tester. High-speed signals are generated and received by Xilinx "GTX" multi-Gigabit transceiver logic. The particular FPGA used in the prototype has 16 TX and 16 RX fully-differential ports, each capable of supporting signals up to 13Gbps.

While the FPGA is very good at generating and receiving multi-Gbps serial test patterns, it has limited ability to vary the test signal analog characteristics, such as voltage amplitude, offset, time-delay, signal pre-emphasis, etc. Therefore, to complement the FPGA and provide a wider range of signal variation, pin electronics (PE) modules are added to the signal paths. For the prototype, a PE module was designed that includes all the electronics for four bidirectional multi-Gbps signals. Multi-pin connectors are arranged near the top edge of the PCB for attaching 16 of these PE

Table 5: 4-CHANNEL PE MODULE PERFORMANCE CHARACTERISTICS

| | |
|------------------------------|--|
| Number of channels | 4 |
| Maximum data rate (DNRZ) | 5.0Gbps |
| Driver rise-time(20-80%) | 45ps (typical) |
| Driver amplitude range | 100mV to 1000mV (single-ended) |
| Driver DC offset range | -0.2V to +1.2V |
| Driver pre-emphasis control | 5-bit digital, including amplitude and duaration |
| Comparator input sensitivity | <10mV (typically <5mV) |
| Comparator range | 0V to 2.5V |
| Delay resolution(lsb) | 5ps |
| Delay range | 5000ps (5ns) |
| Random jitter | 1ps (typical, limited by reference clock jitter) |
| Deterministic jitter | <5ps |
| Transmission line bandwidth | >5GHz |

modules, for a total of 64 channels. During the development phase only four of the 16 PE modules were actually populated on the prototype PCB. Nevertheless, all 16 positions are shown to illustrate the feasibility of scaling up to the full 64-channel test system. In the photograph (Figure 37(b)) the four active PE card connectors are visible just above the FPGA with a single PE card actually present in one of them. The patent-pending design of the PE module includes signal drivers (Tx), receivers (Rx), samplers, signal conditioners, programmable delay elements, serial DACs, relays (for connecting to the host ATE parametric measurement units and low-speed test electronics), and high-bandwidth connectors (for passing the signals between the module and the FPGA and the DUT). Using only off-the-shelf components, the 4-channel PE module is able to accurately produce and measure signals up to 5 Gbps. Other performance characteristics are listed in Table 5.

To illustrate the pin electronics driver characteristics, a multi-gigabit-per-second serial data pattern is generated by the FPGA GTX circuitry and passed to a PE module. After adjusting its delay and voltage characteristics the resulting data "eye" diagrams are shown in Figure 38, using an Agilent 81600D sampling oscilloscope

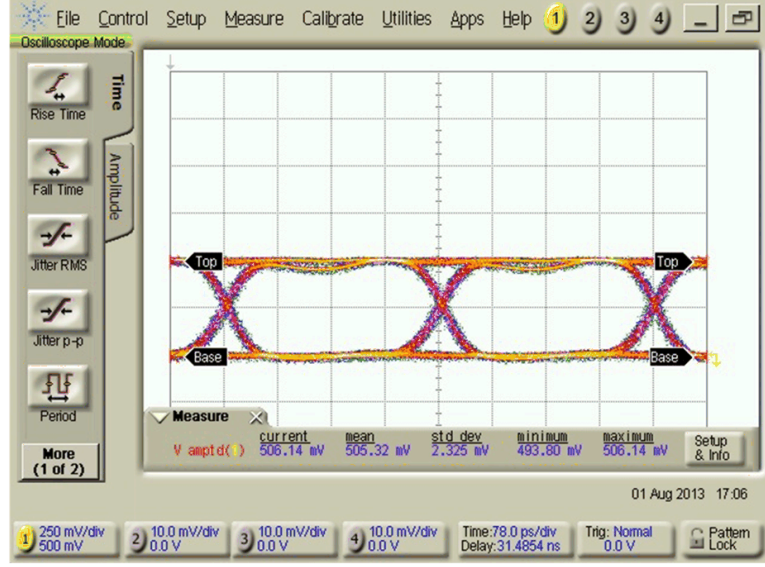
with a 50 GHz bandwidth sampling head. The top figure (Figure 38(a)) shows the signal at 3.2Gbps, and Figure 38(b) shows it at 5.0Gbps. In each case, the pre-emphasis characteristics (duration and amplitude) of the drive signal are adjusted in order to obtain the optimal eye shape at the receiving end of the transmission line (at the oscilloscope input in this case). The pin electronics channels support multiple receiver/sampler circuits that support characterization tests in parallel with functional testing. This allows the driver and DUT signals to be checked while running normal functional tests as well as during offline testing (for set-up, calibration, and signal optimization).

5.2.3 Eye Reconstruction Algorithm by Monobit-receiver

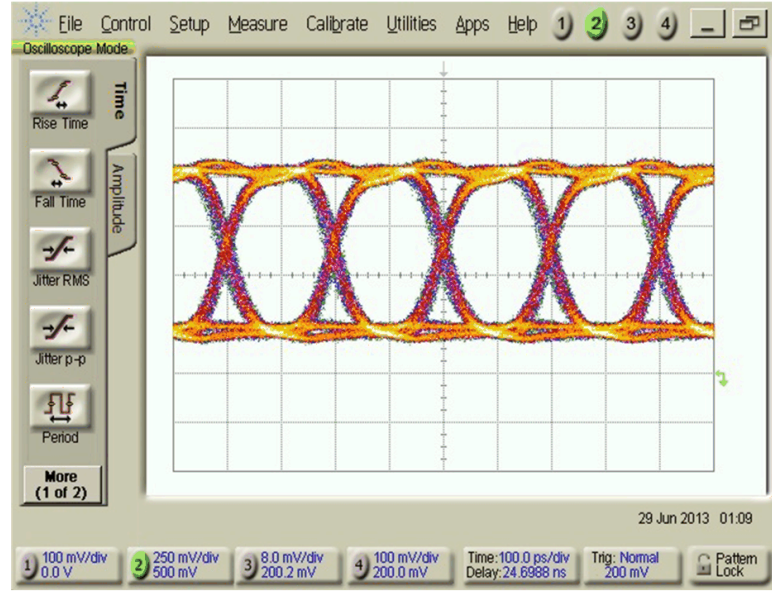
5.2.3.1 *Estimate the fundamental discrete frequency*

In [49, 55], the synchronized sampling clock is time-delayed to sample the different parts of the signal within the bit-period. However, the quality and the time-resolution of the reconstruction are limited by the accuracy of the delay IC. In this paper, the synchronized fractional subsampling is proposed. A fine time-resolution of the reconstruction is achieved by the frequency offset between the sampling clock and the input signal. The time-resolution can be configurable by changing the fractional relationship.

In Figure 39(a), one example of the synchronized fractional subsampling is shown. In this example, the bit-period of the input signal and the period of the subsampling clock has 4/5 relationship. As the input signal and the sampling clock are synchronized, the phase between them is not drifting over the time. Moreover, the phase changes with a period of 4 due to the fractional relationship. Therefore, the synchronization and the fractional relationship create periodic phase offset over the time. In general, when the frequency relationship between the sampling clock (f_s) and the



(a)



(b)

Figure 38: Pin electronics (PE) card driver output data eyes, (a) 3.2Gbps at 78ps/div, (b) 5.0 Gbps at 100ps/div.

input signal (f_c) is as following,

$$f_s = \frac{C}{D} f_c, \quad (78)$$

where C and D are coprime, then is the number of the sampling time-location. Thus,

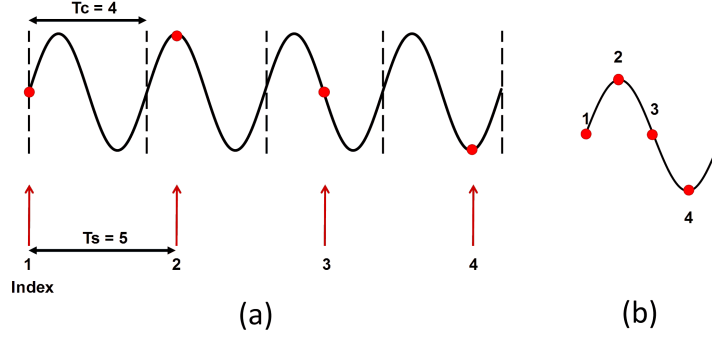


Figure 39: (a) Synchronized fractional subsampling, and (b) its reconstructed waveform.

the time-resolution of the reconstruction is configurable by changing the frequency relationship. We refer D as the subsampling factor. It is also notable that there are infinitely many choices for the frequency of the sampling clock with a given desired time-resolution because D is independent with the resolution. In Figure 39(b), the samples over the period are gathered and the signal is reconstructed by plotting the samples in proper index order.

5.2.3.2 Monobit Eye-reconstruction: Logic Distribution

In this proposed testing system, a monobit clocked-comparator performs as the monobit receiver. The monobit clocked-comparator compares the input signal and the threshold voltage level at the rising edge of the sampling clock. If the input signal is higher than the threshold at the clock edge, the clocked-comparator outputs a logic one. Otherwise, the output is a logic zero.

The reconstruction of the eye-diagram is achieved by adjusting the sampling point and accumulating the output logics from the clocked-comparator. The sampling location can be configured by the combination of the synchronized fractional subsampling and the programmable threshold voltage. In Figure 40, different sampling points are shown for five threshold levels and three sampling locations ($C = 3$). The sampling point (p1 p5) is adjusted by the programmable threshold voltage ($Th =$

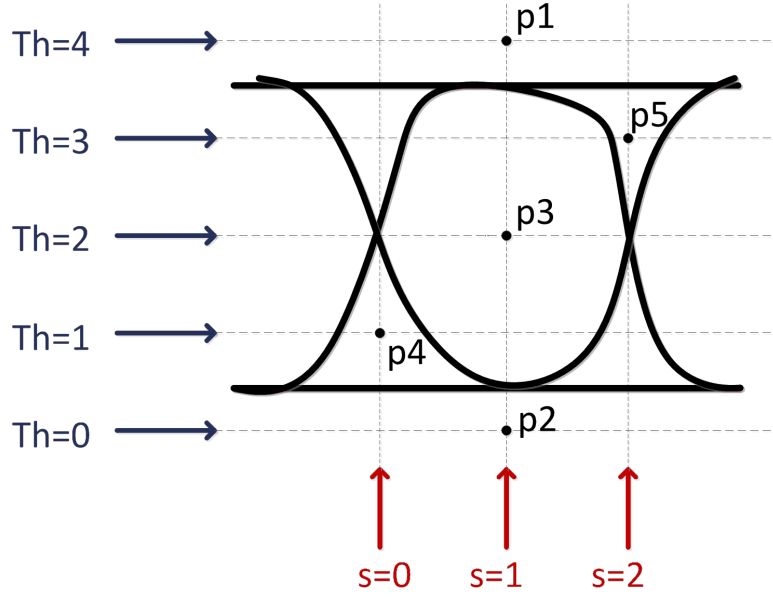


Figure 40: Different sampling points in eye diagram by adjustable threshold level and synchronized fractional subsampling.

0 4) and the dynamic sampling clock-edge ($s = 0 \ 2$) due to the synchronized fractional sampling. Note that the location of the sampling clock-edge is periodic with C (i.e., $1- > 0- > 2- > 1- > 0- > 2- > \dots$). If the sample point is above the high level of the input signal (p1) or below the low level of the input signal (p2), the output logic of the clocked-comparator is always zero (p1) or one (p2). However, if the sample point is within the high and the low voltage level (p3, p4, and p5), the output logic is not deterministic. The outcomes of the logic depend on the statistics of the bit pattern. In this paper, we assume the input signal is a PRBS whose logic transition is balanced. This means that the number of the four possible logic-transitions (one-to-one, one-to-zero, zero-to-zero, zero-to-one) is equally distributed in a long observation. With this assumption, the distribution of logic one and zero at p3 is expected to be 1:1. It is because the sample point (p3) is below the two logic-transitions (one-to-one and one-to-zero) and above the others (zero-to-zero and zero-to-one). Likewise, the logic distribution at p4 and p5 is expected to be 3:1 and 1:3, respectively. Therefore, the shape of the eye can be distinguished by the logic

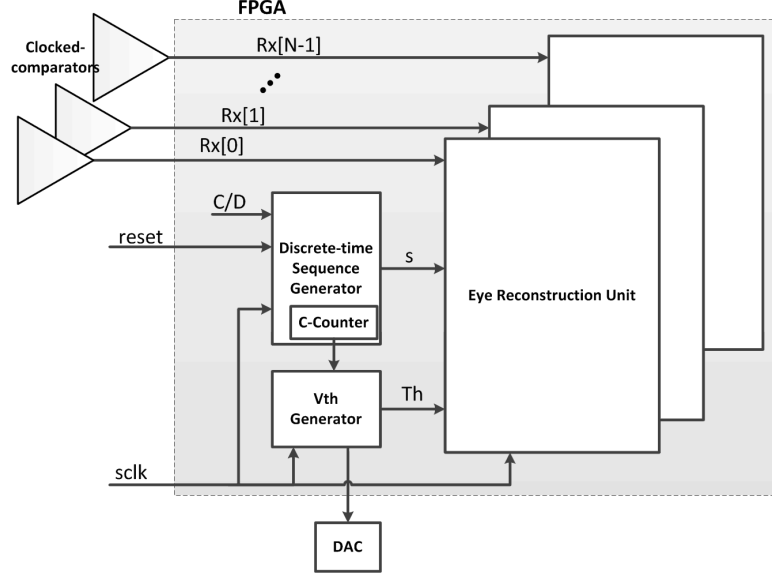


Figure 41: Block diagram of FPGA logic.

distribution.

5.2.3.3 FPGA Logic

The monobit eye-reconstruction algorithm is implemented in FPGA logic. The block diagram of the FPGA logic is shown in Figure 41. The current sampling location is tracked and stored by updating a sequence every sampling clock (Discrete-time sequence generator). As described in the previous section, the time-location of the sampling clock-edge forms a periodic sequence depending on the frequency relationship parameterized by coprime C and D . In order to accumulate a logic distribution at a point, the corresponding threshold is fixed until a desired amount of the logics at the point is gathered. For example, to obtain the logic distribution at point p_3 with 10 logic-samples, the threshold is fixed at level 2 for 30 cycles ($3 \cdot 10$). The parameter C is multiplied due to the periodicity of the sampling location (C-Counter). After the desired number of the samples are collected, the threshold is programmed to the next level (Vth generator). The logic distribution at each evaluated point is stored in the memory (Eye reconstruction unit).

The accuracy of the eye-reconstruction depends on 1) the time-resolution (C), 2) the number of threshold level (NTh), and 3) the number of logic-samples (L) for each sampling point. If the entire eye reconstruction is required, the total amount of memory will be $C \cdot NTh \cdot \lceil \log_2 L \rceil$ bits. Therefore, there is a tradeoff between the accuracy and the amount of resource.

5.2.4 Hardware Experiment

The FPGA generates 3.2Gbps NRZ PRBS test signal (length of sequence = $2^7 - 1$) and receives the output logic from the clocked-comparator. The sampling clock for the clocked comparator and the FPGA logic is chosen to have sampling time-location over the bit period ($1/f_b$) of the PRBS. We also choose $D = 3200 \cdot 10$ for the subsampling factor, and the resulting sampling frequency would be

$$f_s = \frac{C}{D} f_b = \frac{313}{3200 \cdot 10} \cdot 3.2\text{GHz} = 31.3\text{MHz}. \quad (79)$$

In this setup, sub-picosecond resolution (0.9984ps) can be achieved.

In Figure 42, the reconstructed eye-diagrams are compared with the input PRBS captured by an Agilent 81600D sampling oscilloscope. The reconstructed eye-diagrams are obtained by $Nth = 121$ threshold level with 0.6mV step and $L = 128$ number of logic-samples per a sample point. The FPGA stores the reconstructed eye-diagram in 313-by-121 array. To visualize the resulting logic distribution, the array is color-mapped. The driver is programmed with three different pre-emphasis. Figure 42(a) compares the input signal without pre-emphasis and the corresponding reconstruction. Figure 42(b) shows the input signal with 15% pre-emphasis magnitude and 100ps pre-emphasis duration and the corresponding result. Figure 42(c) shows the input signal with 25% pre-emphasis magnitude and 200ps pre-emphasis duration and the corresponding result. The shapes of the reconstructed eye-diagram correspond well to the corresponding input waveform. For example, the pre/post transition overshoot and undershoot in the input waveform of Figure 42(a) is presented in the

corresponding reconstructed eye-diagram. Similarly, the input signal in Figure 42(c) is over pre-emphasized and its signal shape is tracked in the reconstruction. In this experiment, we can find the optimal pre-emphasis (Figure 42(b)) by the reconstructed eye-diagram.

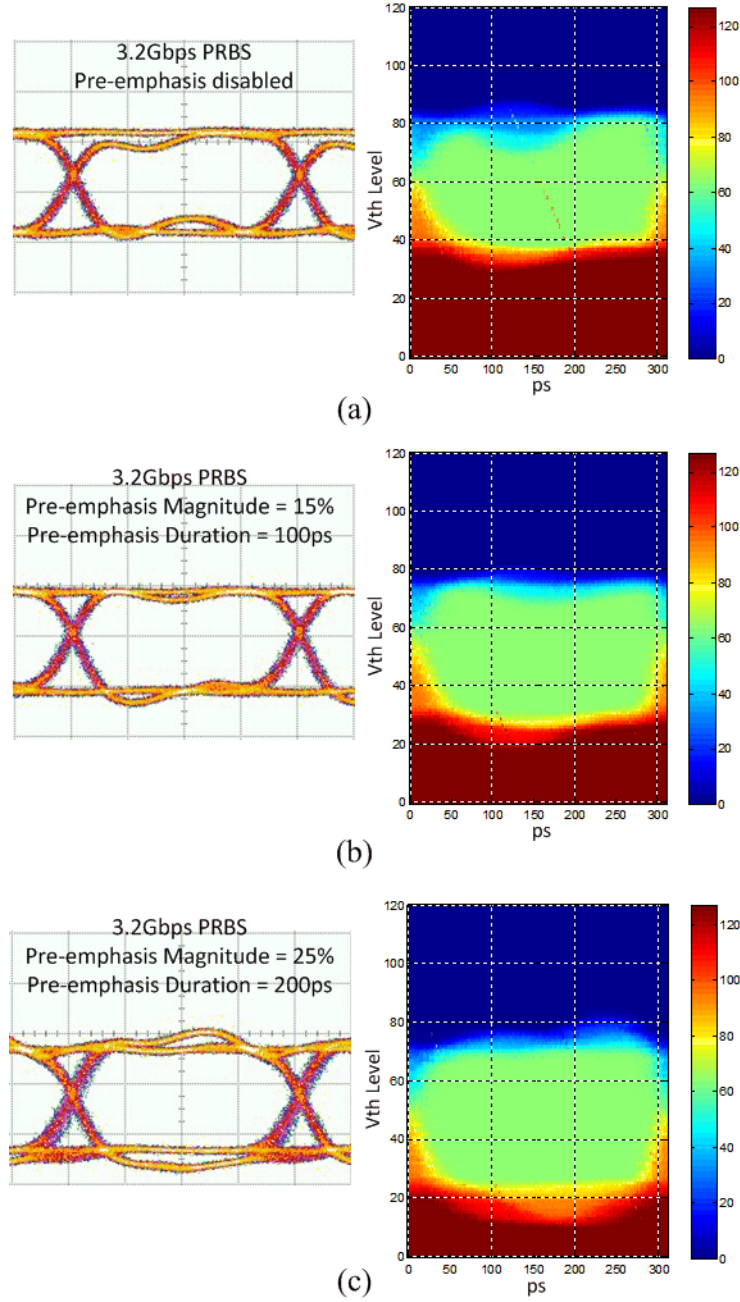


Figure 42: 3.2Gbps PRBS input waveforms and reconstructed eye-diagrams for three different pre-emphasis settings of the driver.

In Figure 43, the typical rise and fall times and peak-to-peak jitter of the input signal are shown with the edge-highlighted reconstructed eye-diagram of Figure 42(b). With a proper voltage swing and DC-offset at 3.2Gbps throughput, rise and fall times are typically about 45ps (20% 80%) and peak-to-peak jitter is about 30ps including 6s random jitter. As shown in Figure 43, the reconstructed eye-diagram is able to represent the timing-characteristics of the input signal.

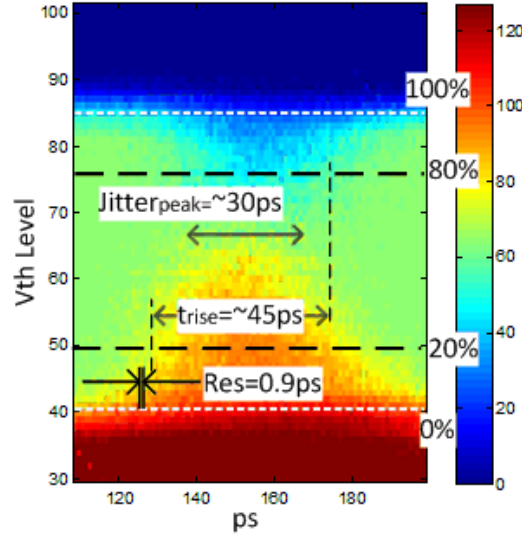


Figure 43: Typical rise and fall times and peak-to-peak jitter of the input signal and reconstructed eye-diagram.

5.2.5 Conclusion and future work

In this paper, we present a new multi-channel testing architecture for high-speed eye-diagram. The combined use of pin electronics and FPGA implementable reconstruction algorithm achieves sub-picosecond resolution for multi-Gbps eye-reconstruction with subsampling clock as well as high scalability of test system. The hardware measurement result verifies the reconstructed eye-diagram is well matched with the input waveform. In our future work, a robust method to quantify the characteristics of reconstructed eye-diagram will be presented.

5.3 Monobit Signal Acquisition and Transient Response Tuning of High-speed Serial I/O Systems

The recent trend for faster devices and high-volume data storage increases demands on high-speed interconnections. The degradation of the high-speed signal, such as attenuation, ringing, reflection and crosstalk, is now important issues. According to [2], it is reported that the reasons for majority of the signal degradation are high-speed interconnects.

To mitigate the high-speed signal degradation and intersymbol interference (ISI), various equalization techniques have been considered. In the receiver front-end, continuous-time linear equalizers (CTLE) and decision feedback equalizers are commonly employed to compensate for the signal distortions and loss. Tuning the filter coefficients and implementing adaptive sampling in the receiver can be achieved because the channel information is captured by the samples. However, tuning the equalization in the transmitter is not straightforward unless an extra physical link conveys the channel information from the receiver. In [74], the optimal equalizer coefficients of transmitter is obtained through a physical feedback line by handshaking with an adaptation logic in receiver. In [34, 54], the strength of pre-emphasis is determined by estimating the channel length. While the channel length is calculated by the time of flight measured by an extra physical line forming a loop in [34], an adaptive pre-emphasis calibration scheme based on the time-domain reflectometry (TDR) is proposed in [54]. These works, however, consider only the channel length as the reason for the signal degradation.

In this paper, a new transient response tuning scheme is proposed for high-speed serial transceiver without an extra physical line. By the proposed scheme, a full TDR waveform is reconstructed by a robust monobit reconstruction algorithm and the impedance discontinuity causing reflections between the transceiver is detected. Once the location, the type, and the quantity of the faults are determined, the signal

degradation in the receiver can be predicted and can be compensated by pre-emphasis of the transmitter.

Various researches to detect wiring/transmission line fault have been studied. In [54, 59], joint time-frequency domain reflectometry (TFDR) technique to detect multiple faults accurately is proposed. However, these works require a high-speed arbitrary waveform generator (AWG) to generate a chirp signal and a wideband circulator to isolate the reflected signal from the fault. In [58], spread spectrum time domain reflectometry (SSTDR) and sequence time domain reflectometry (STDR) are proposed. A spread spectrum signal is injected onto the wires and the observed reflected signal is correlated with a copy of the injected signal to detect the faults. This approach, however, demand a pair of duplicated pseudo-noise digital sequence generators and a correlator which is composed of a wideband mixer and an integrator circuit. Therefore, these approaches are not adequate and cost-efficient for diagnosing faults in digital high-speed interconnection due to extra signal generators and special circuitry.

In this work, the proposed test architecture uses field programmable gate arrays (FPGAs) for pattern synthesis and sample acquisition. The FPGA logic is complemented by customized pin electronics (PE) modules including high-speed drivers and comparators. As FPGAs are capable of multi-channel IOs and the PE modules are constructed using off-the-shelf components, the cost of the test module is minimized as well as the multi-channel high-speed testing is achieved. Moreover, a novel algorithm that reconstructs a full TDR waveform without extra timing circuitry and a new approach diagnosing multiple faults in the channel achieves a robust channel monitoring while minimizing hardware cost. The contribution of this work can be summarized as:

- A new monobit test architecture and a dedicated reconstruction algorithm reduce the testing cost compared to the conventional approaches.

- Multiple faults can be detected and diagnosed by our impedance reconstruction algorithm.
- By the proposed approach, the high-speed transmitter is able to be tuned without communicating with the receiver.

5.3.1 Monobit Signal Reconstruction

5.3.1.1 Monobit Fractional Equivalent Sub-sampling

A waveform is reconstructed in the time-domain by two different approaches: real-time sampling (RTS) and equivalent-time sampling (ETS) [9]. While the RTS plots the samples in sequence, the ETS reconstructs the waveform by re-ordering the samples over the period of the waveform. The ETS is commonly used to scope a high-speed digital waveform over the RTS because the ETS can take advantage of sub-sampling due to the periodicity of the digital waveform whereas RTS can suffer from the aliasing issue.

The conventional ETS varies the sample delay to sweep across the waveform. The sample delay is sequentially increasing by ΔT to sample across the waveform. However, the resolution of the reconstruction is limited by the minimum amount of the sample delay. In [45], fractional equivalent-time sampling (FETS) is introduced. Compared to the conventional ETS where both sampling clock and the input share the same frequency or an integer relationship, the FETS uses a frequency offset between the sampling clock and the input waveform. In Figure 44, the conventional ETS and the FETS are compared. In the example of the conventional ETS, the sampling clock has the same frequency with the input waveform ($T_s = T_c$). In general, the frequency of the input waveform (T_c) is integer multiple of that of the sampling clock (T_s). On the other hand, the sampling frequency in FETS has fractional relationship with the input waveform. Because of the fractional relationship, a periodic phase offset is created over the input waveform.

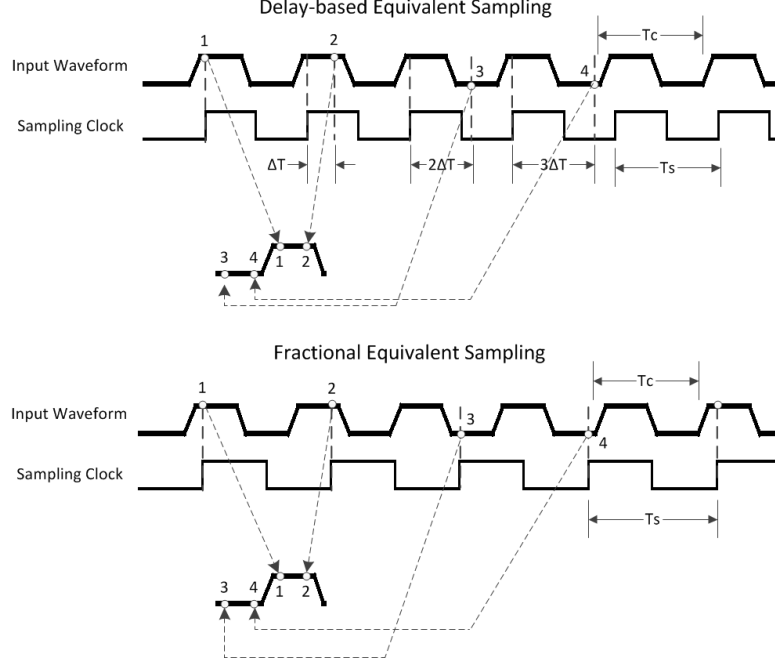


Figure 44: Conventional ETS (above) and fractional ETS (below).

To generalize, we define the frequency relationship between the sampling clock ($f_s = 1/T_s$) and the input waveform ($f_c = 1/T_c$) as following

$$f_s = \frac{n}{m} f_c, \quad (80)$$

where m and n are coprime. Then, the total number of the sampling time-location (or the resolution of the reconstruction) is n . Thus, the time-resolution of the reconstruction is configurable by changing the frequency relationship. There are infinitely many choices of the frequency relationship given a time-resolution because m is independent with the resolution. The sequence of the sampling time-location is defined as

$$s[k] = \text{mod}(kT_s, T_c). \quad (81)$$

The sequence, $s[k]$, contains a relative phase information of k -th sample. When the sampling clock and the input waveform hold the relationship as (80), the sampling time-location can be expressed in integer rather than in real number. The definition

can be re-defined as

$$s[k] = \text{mod}(km, n). \quad (82)$$

In the proposed testing system, a clocked-comparator performs as a monobit receiver. The input waveform and the threshold voltage level are compared at the rising edge of the sampling clock. When the input signal is higher than the threshold at the clock edge, the comparator outputs a logic one. Otherwise, the comparator outputs a logic zero.

The reconstruction by monobit sampler is achieved by the combination of FETS and varying the threshold level. As discussed in earlier, the phase of the sampling clock sweeps across the input waveform. In Figure45, 30 different sampling points are formed by 6 threshold levels and 5 clock edges ($n = 5$) as an example. Note that the phase of the sampling-clock-edge is periodic with n but the sequence does not have to be in order. The threshold level is sequentially increased by every n clock-cycles. The output logic of the comparator is sampled and stored in FPGA corresponding to the sampling point. In Figure45, the output logics are shown for a square waveform. The figure illustrates that the original waveform seats between the boundary of the logic '1' and '0'. One of the naive approach to reconstruct the waveform is taking 'median' of the logic boundary. In this example, the reconstructed waveform by this approach will be $\{0.5, 0.5, 2.5, 4.5, 4.5\}$. However, a robust signal reconstruction algorithm is desired in the presence of white Gaussian noise in the input waveform and the threshold voltage and jitter noise in both of the input waveform and the sampling clock. In the next section, a robust signal reconstruction algorithm based on the proposed monobit FETS is described.

5.3.1.2 Robust Monobit Reconstruction

Unlike a multi-bit resolution ADC, a monobit receiver provides boolean-type information whether a waveform is greater or less than a given threshold value. We first

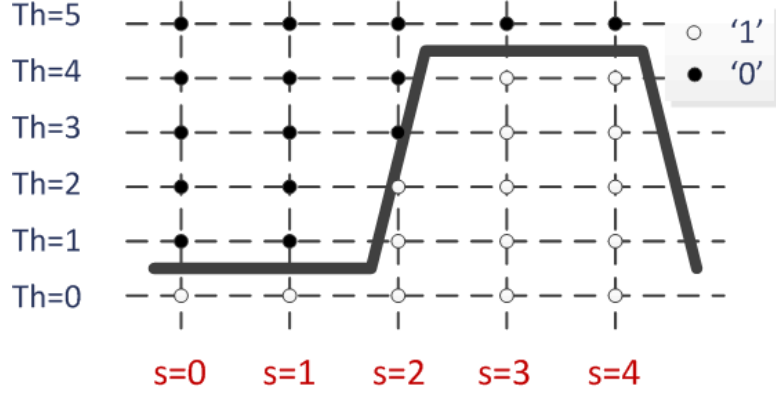


Figure 45: Monobit subsampling.

assume that the sample noise is white Gaussian. For simplicity's sake, we fix the sampling-clock-edge and only consider the samples given by different threshold levels. The input waveform in the presence of noise is described as

$$Y_i \sim N(\mathbf{x}, \sigma^2), \quad (83)$$

where \mathbf{x} is the original input waveform and σ is the standard deviation of the white Gaussian noise. The independent and identically distributed (i.i.d.) random samples Y_1, Y_2, \dots, Y_N can be thought as samples from a multi-bit resolution ADC. In monobit receiver, however, the outcome of the samples is boolean. Thus, the random sample of monobit receiver is

$$Z_i = \begin{cases} 0 & , \quad Y_i < \beta_i, \\ 1 & , \quad Y_i \geq \beta_i, \end{cases} \quad (84)$$

where β_i is the i -th threshold level. Figure 46 shows an example of the waveform at \mathbf{x} with the normal distributed noise. Let N -number of the observed sample values be $D = [d_1, d_2, \dots, d_N]$, $d_i \in \{0, 1\}$ and the parameters to be estimated be $\theta = \{\mathbf{x}, \sigma^2\}$.

An intuitive and naive way to estimate the original waveform is taking the median of the min/max threshold of the logic '1' and '0'. In Figure 45, one can find that the original waveform lies between the minimum threshold of the logic '0' and the

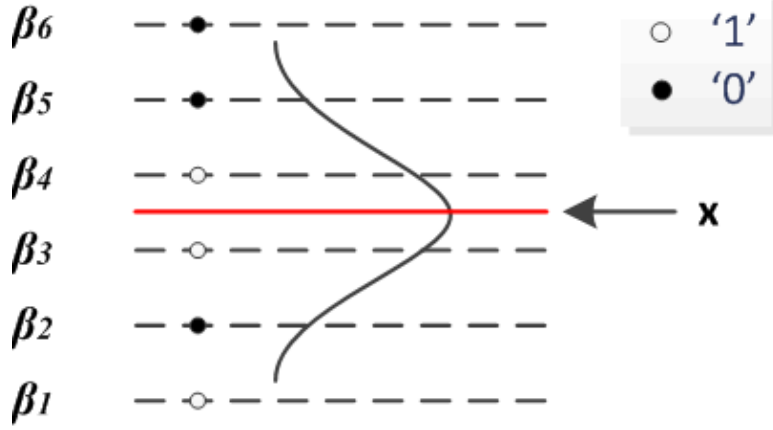


Figure 46: The threshold levels, the original signal level (red cross line), and its noise distribution.

maximum threshold of the logic '1' for each sampling time-location. The estimation of \mathbf{x} by median is

$$\hat{\mathbf{x}}_{median} = \text{median}(\max_{Z_i=1} \beta_i, \min_{Z_i=0} \beta_i). \quad (85)$$

The likelihood function is defined as

$$L(\theta) = \mathbf{Pr}(D|\theta) \quad (86)$$

$$= \mathbf{Pr}(Z_1 = d_1|\theta) \mathbf{Pr}(Z_2 = d_2|\theta) \cdots \mathbf{Pr}(Z_N = d_N|\theta) \quad (87)$$

$$= \prod_{i=1}^N \mathbf{Pr}(Z_i = d_i|\theta) \quad (88)$$

$$= \prod_{i=1}^N \mathbf{Pr}(Y_i < (-1)^{d_i} \beta_i|\theta). \quad (89)$$

The likelihood function states that the probability of the observations (D) given the parameter (θ). Note that the observations give us the one-sided range of the random samples. Therefore, the likelihood function is composed of the cumulative distribution function (CDF) of the normal distribution. Since the natural log function is one-to-one and monotonically increasing, it is more convenient to use the logarithm of the likelihood function defined by

$$\ln L(\theta) = \sum_{i=1}^N \ln \mathbf{Pr}(Y_i < (-1)^{d_i} \beta_i|\theta). \quad (90)$$

The maximum likelihood estimator (MLE) of θ is the value of θ that maximizes $\ln L(\theta)$.

$$\hat{\theta}_{MLE} = \arg \max_{\theta} \ln L(\theta). \quad (91)$$

As there does not exist a closed form of the CDF for the normal distribution, the MLE of θ is found by a numerical approach. In our case, the CDF of normal distribution can be easily evaluated by the standard normal distribution table or any computer tools for statistics.

Consider an example with $Y_i \sim N(0, 1)$. The random samples are evaluated with $N = 100$ different threshold levels (β) linearly spaced by 0.1 and centered at 0. Figure 47(a) shows the boolean outcomes of the comparator. Since there are two parameters (\mathbf{x}, σ) to be estimated, the likelihood function is evaluated by sweeping both parameters. Figure 47(b) shows the logarithm of the likelihood function with respect to \mathbf{x} and σ . In this example, the maximum value is at the point of $\hat{\mathbf{x}} = 0$ and $\hat{\sigma} = 1.05$. The result shows that the MLE gives very close estimations to the true values. In Figure 47(c), the same results are projected across $\hat{\sigma}$. As one can see, the plot has the maximum around $\hat{\mathbf{x}} = 0$ for each $\hat{\sigma}$. As we are more interested in estimating \mathbf{x} than σ , this observation suggest that the MLE of \mathbf{x} is not too sensitive to that of σ . In other words, we may compute the MLE over one parameter (\mathbf{x}) by fixing the other (σ) at an arbitrary value. However, choosing a fixed σ requires careful considerations because overestimated σ can force the likelihood function to be flat over \mathbf{x} and results in a mislead estimation.

In Figure 48(a), a clock waveform as TDR stimulus is simulated with noise and jitter. The waveform has 1V amplitude with noise of standard deviation $\sigma = 0.08$. The reconstruction waveforms by median and MLE are shown in Figure 48(b). Both of the reconstructions are fairly close to the original waveform but MLE has closer reconstruction to the original. The mean squared error between the reconstruction and the original waveform is compared in Figure 48(c). The bar graph provides

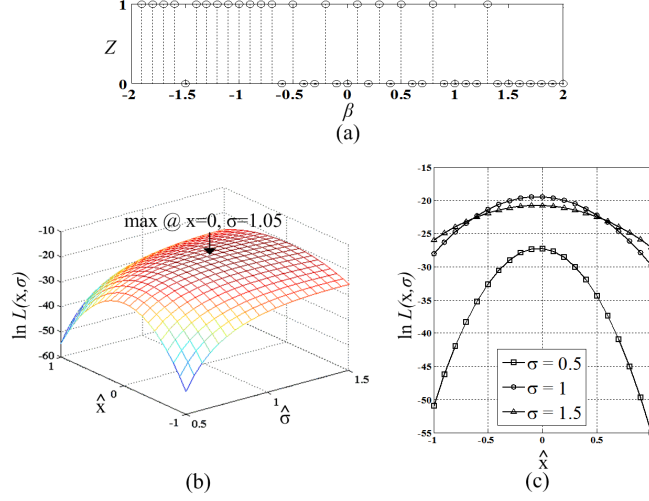


Figure 47: (a) The boolean outputs of the comparator across the threshold levels (b) The logarithm of the likelihood function with respect to mean and standard deviation. (c) The projected logarithm likelihood function.

us that MLE can reduce the error more rapidly than median estimation with the accumulated samples. A single iteration means the full samples over the sampling time and the threshold level (i.e. 5-by-6 samples in Figure 45). This is because median estimation only uses the two extreme samples which are rarely updated over the time while MLE can exploit the samples between the two points.

5.3.2 Adaptive Pre-emphasis by TDR

We consider a specific problem of monitoring multiple faults in a transmission line using time domain reflectometry (TDR) and tuning the pre-emphasis of transmitter to compensate the degradation of the eye-diagram at the receiver. A TDR is connected to the transmission line under test and launches a known signal down the line. A reflected waveform is monitored to detect the faults in the transmission line. The faults are categorized as hard faults and soft faults. The hard faults refer to open or short circuits and results in an abrupt changes of the TDR waveform. An open-circuited line doubles the incident waveform and a short-circuited line cancels the incident waveform. Therefore, detecting hard faults in a point-to-point line is evident. On

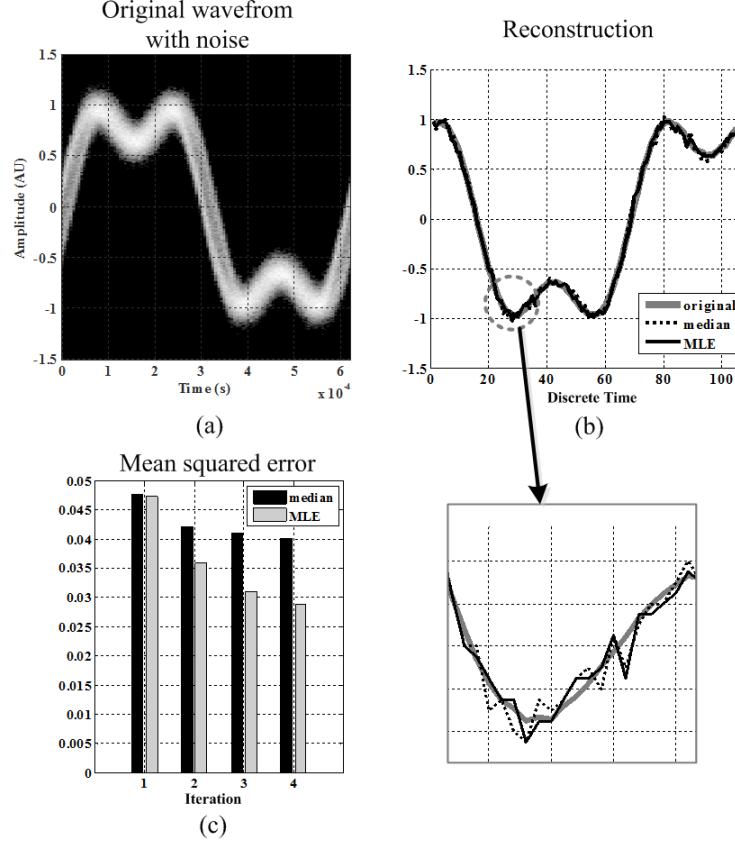


Figure 48: (a) Input waveform (b) The reconstructions by median and MLE. (c) The mean squared error comparing median and MLE.

the other hand, any faults other than open or short circuits can be classified into soft faults. Soft faults result from a spatially continuous variations of certain parameters of the transmission line or capacitive/inductive impedance discontinuities due to connectors or vias. In this paper, the considered soft faults correspond to capacitive and inductive impedance discontinuities. When a single fault is assumed, the fault can be diagnosed by a closed form [6, 28, 77]. However, locating and measuring multiple faults in the transmission line is challenging because of multiple reflections and degradation of the incident signal as it propagates through the multiple faults. To resolve the impedance profile of a nonuniform transmission line, [26, 36] proposed a recursive computation method. This method, however, has stability issues with general incident signal other than step-function. Moreover, these TDR analysis algorithms

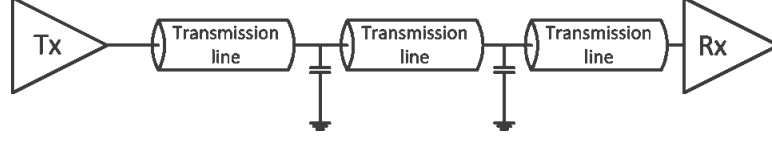


Figure 49: An example of the channel with multiple capacitive faults.

require the computational burden that the real-time adaptation is not applicable.

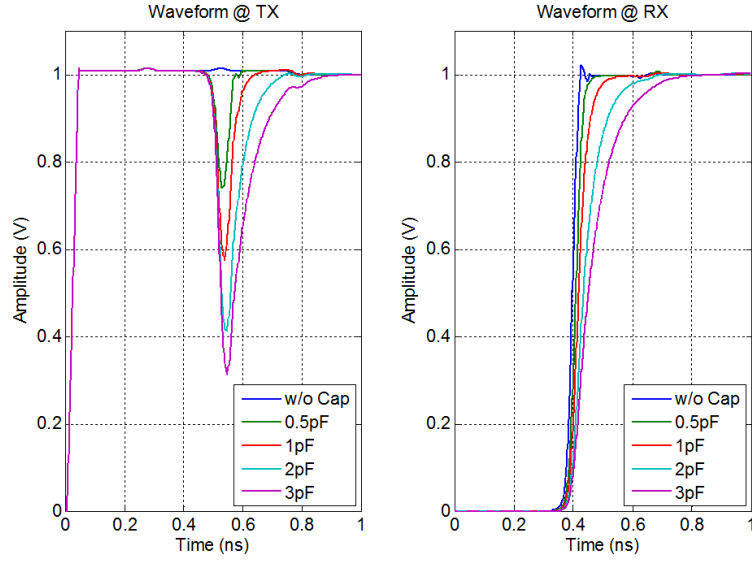
In this section, a new adaptive pre-emphasis self-calibration using TDR waveform is proposed. The pre-emphasis strength is self-calibrated by monitoring the channel using the monobit signal acquisition in the previous section. Thus, the calibration is achieved without any extra feedback line from the receiver.

The soft faults are assumed to be one or more in the channel as shown in Figure 49. The distance between the faults are assumed to be large enough so that the reflected waveform does not overlapped. A computer simulation by Advanced Design System is performed for a single capacitive fault. In Figure 50, the TDR waveforms (or the waveforms at the transmitter) and the waveforms at the receiver are shown with different amount of capacitors in the channel. A larger capacitor generates a stronger reflection at the transmitter and a slower rising-time at the receiver. The lagging effect on the receiver due to the impedance mismatch degrades the signal integrity such as eye-diagram. Therefore, monitoring the channel before transmitting the data and adapting the pre-emphasis will enhance the transceiver performance. Note that the rising-time at the transmitter also affects the rising-time at the receiver. In Figure 50(a), the incident step waveform is a ramp signal with 24ps rise-time(20-80%). The incident waveform with doubled rise-time (48ps) is illustrated in Figure 50(b).

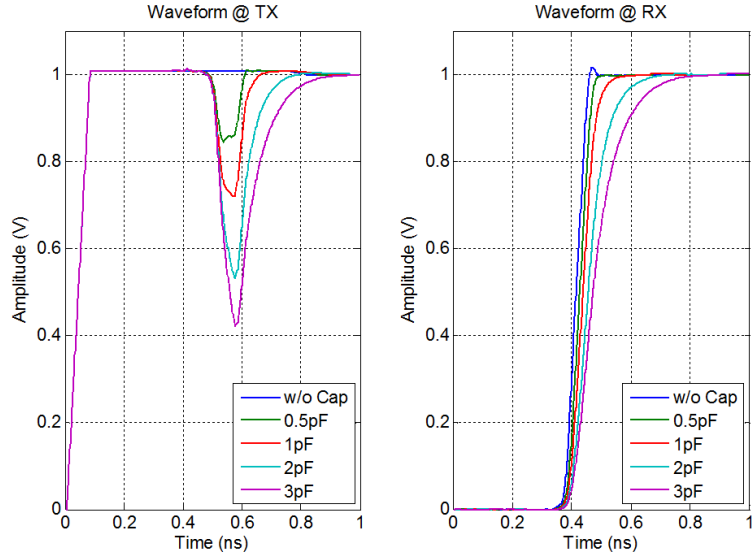
The amount of the reflection can be measured by integrating the absolute value of the reflected waveform as

$$\alpha = \int_0^{\infty} |V_{tdr}(t) - V_{ref}(t)| dt, \quad (92)$$

where V_{ref} is the TDR waveform without any reflections. The ratio of the rise-time at the receiver (RTr) and the rise-time at the transmitter (RTr) is denoted by ρ . The



(a)



(b)

Figure 50: The TDR waveform (left) and the waveform at the receiver (right) with various soft-faults for (a) 24ps RTt and (b) 48ps RTt.

relation between the ratio (ρ) of the rise-time and the integral of the reflection is plotted in Figure 51. It is shown that the two parameters are approximated in linear relationship. As the impedance mismatch is larger, the stronger reflection will occur. The impedance discontinuity results in degradation of the rise-time at the receiver.

An eye-diagram is an intuitive and easy metric to evaluate the performance of

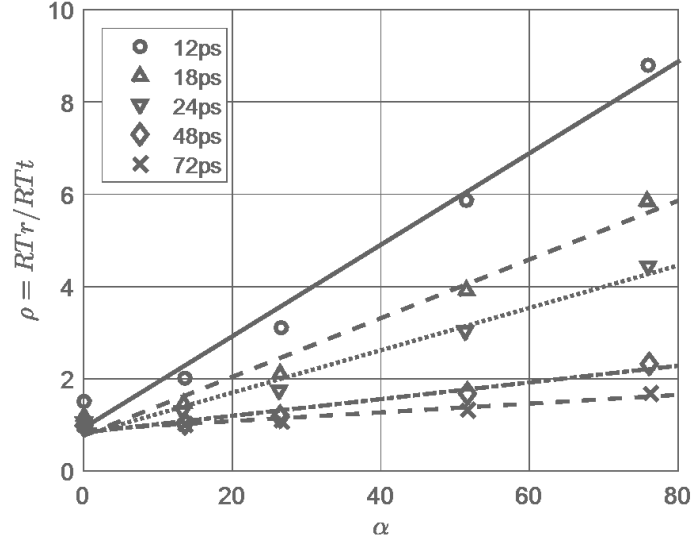


Figure 51: The relationship between the integral of the reflected waveform and the rise-time ratio (RT_r/RT_t) with various RT_t .

a digital signal. As the eye-diagram is usually obtained by overlapping the digital signal over one or two bit period (unit interval), a significant amount of samples and computation time are required to determine a full eye-diagram, which is not suitable for real-time adaptation. In Figure 52, the eye-diagram at the receiver and its eye-opening area are shown. In this paper, the eye-opening area is defined by finding the 7 longest vertical lines equally spaced over the unit interval (UI) and contained in the closed eye area. Then, the sum of the rectangulars whose heights are the vertical lines is the eye-opening area.

The relationship between the rise-time (RT_r) and the eye-opening area is shown in Figure 53. It shows the linear model fits the data well. The strength of the pre-emphasis can be determined depending on the initial condition (eye-opening area without pre-emphasis) and the required compliance eye-opening.

5.3.3 Hardware Measurement

We use a test channel board that emulates transmission line faults. On a transmission line, a combination of shunt capacitors or series inductors can be soldered as shown

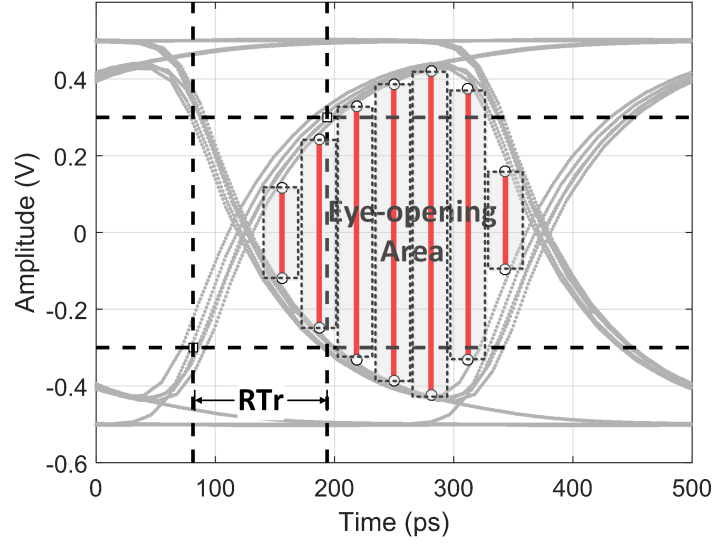


Figure 52: Defined eye-opening area and rise-time (RTr).

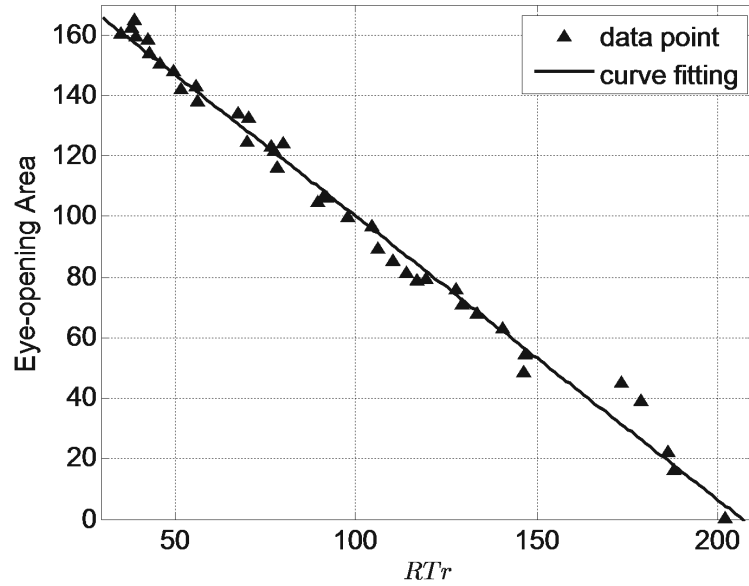


Figure 53: The relationship between the RTr and the eye-opening area.

in Figure 54. In Figure 55, TDR waveforms obtained by the proposed method are compared with Agilent 81600D sampling oscilloscope with a TDR module. In the case without fault (top), there are two voltage drops because the two SMA connectors act as capacitor. In the case with two 1pF capacitors (middle), the reflection due to the first capacitor appears after the first SMA connector. The reflection due to the second

Table 6: POWER CONSUMPTION OF DRIVER AT 3.2GBPS PRBS

| | Disable | 15%, 200ps | 33%, 200ps |
|-------|---------|------------|------------|
| Power | 957mW | 978mW | 991mW |

capacitor overlaps with the one due to the second SMA connector. In the last case with a single inductor, the reflection waveform reinforces the incidence waveform.

As discussed in the previous section, the relationship between the integral of the reflected waveform and the rise-time at the receiver (RTr) (Figure 51) and the relationship between the RTr and the eye-opening area are both approximated in linear model. Therefore, we can expect the integral of the reflected waveform and the eye-opening area can be linear, too.

In Figure 56, the measured TDR reflection area and the eye opening area are plotted together. The optimal pre-emphasis takes the reflection area into account. The reflection area is divided into three ranges in this example. The first range (white) is considered to have low impedance mismatch that the compliance is already met without enabling pre-emphasis. The second range (light grey) starts to having medium amount of impedance mismatch. The eye-diagram does not meet the compliance now, so the pre-emphasis is necessary. However, the maximum strength of the pre-emphasis (33% amplitude, 200ps duration) will give too much eye-opening which wastes redundant power. In this range, the medium strength (15% amplitude, 200ps duration) is enough to meet the compliance. In the third range (dark grey), the channel is suffering high impedance mismatch so that the maximum pre-emphasis is required.

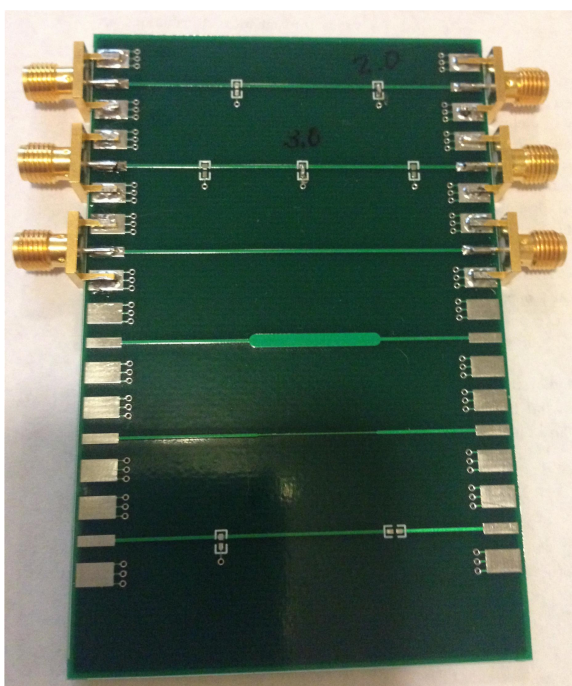


Figure 54: A test channel board.

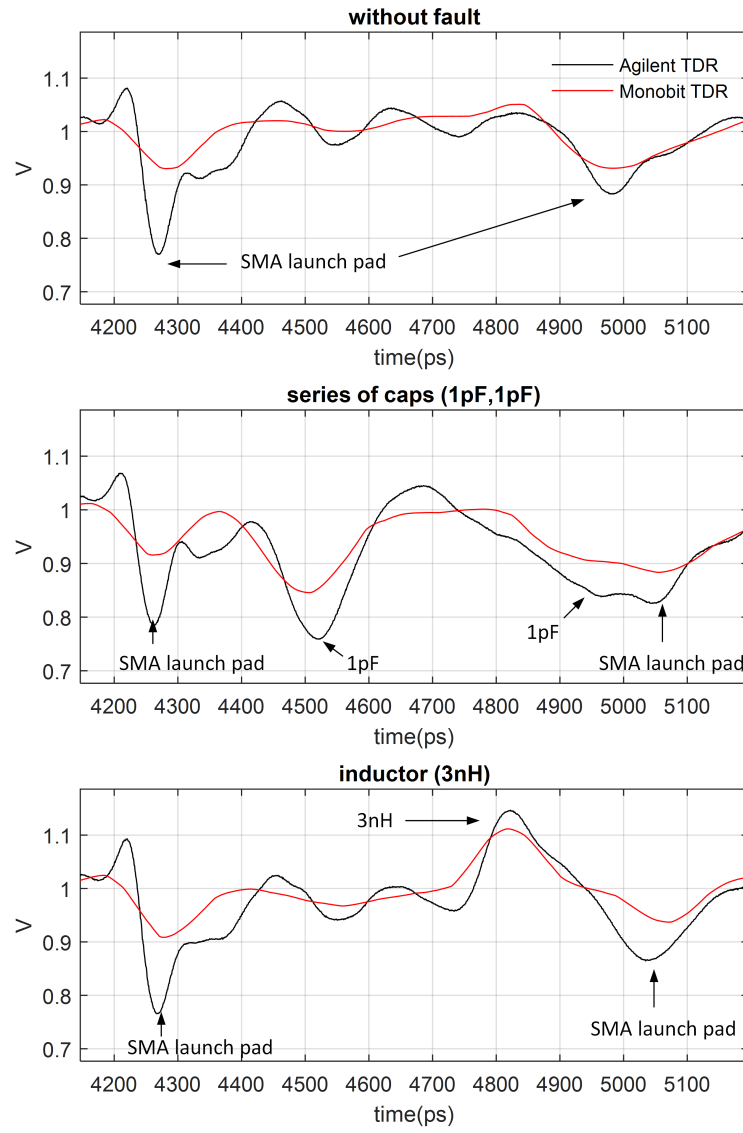


Figure 55: TDR waveforms by Agilent and by proposed work.

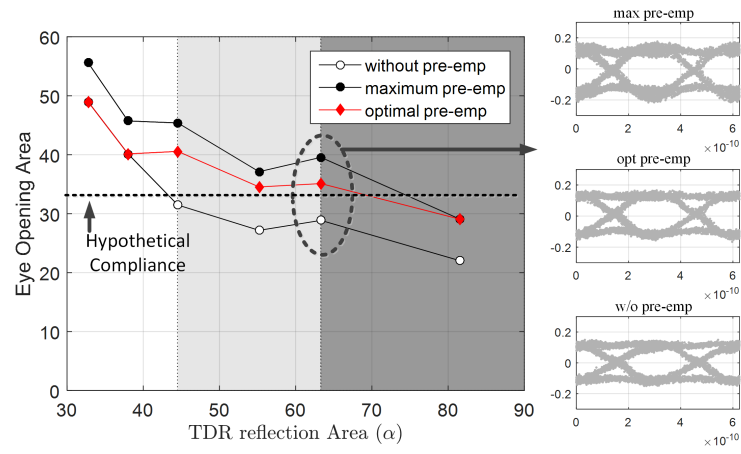


Figure 56: Measured TDR reflection area and eye-opening area.

CHAPTER VI

CONCLUSION

We summarize the main contributions of the dissertation:

- The wideband signal reconstruction is achieved by direct subsampling. The signal distortion and nonlinearity from the RF front-end component are avoided by the proposed approach. The combination of the proposed dual sampling rate signal acquisition testing architecture and multicaset algorithm significantly reduces the number of sampling channel needed in the conventional multicaset works. The optimality of the dual sampling rates is studied and verified by computer simulation. Practical issues of the dual-rate sampling hardware such as phase synchronization and channel mismatch calibration are presented and solved.
- The long-term jitter in PRBS is tracked without hardware synchronization and clock data recovery (CDR) circuits. We proposed an improved algorithmic clock-recovery method using the spectral analysis. The accuracy of the frequency estimation is improved and the computational burden is reduced by sequentially narrowing the bandwidth of the spectral evaluation through multiple analysis steps.
- We proposed various different monobit test architectures and reconstruction algorithms. Using a monobit-receiver and a threshold signal, high resolution of reconstructed signal in both amplitude and time is achieved. Two different reconstruction algorithms are presented whether the threshold signal is synchronized or not. The monobit reconstruction is further enhanced by statistical

estimation. The proposed test architecture is used to perform a TDR on the high-speed channel and adapt the channel condition to improve the eye-diagram by controlling the pre-emphasis coefficients.

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